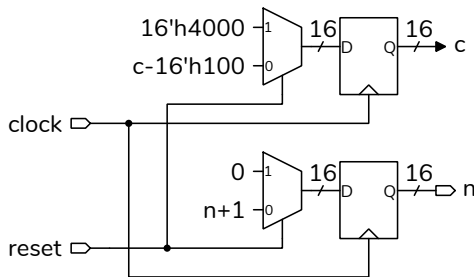# Solutions to Final Exam

There were two versions of each question. The values and the answers for both versions are given below.
Revision 2: Corrected size of `n` in solution to Question 1 and order of answers in Question 2.

Question 1

Write a Verilog module corresponding to the schematic shown below. The module name is `sdiv` (or `adiv`). Include the module declaration and any additional required signal declarations. The diagram below follows the course guidelines for schematics. Follow the course coding conventions but omit comments.

Answers

```verilog
module adiv
  ( input logic clock, reset,
    output logic n [15:0] ) ;

  logic [15:0] c ;
  always_ff @(posedge clock)
    c <= reset ? 16'h4000 : c-16'h100 ;

  always_ff @(posedge clock)
    n <= reset ? '0 : n+1 ;

endmodule
```

The second version has the same answer but with a module name of `adiv`.

Question 2

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```verilog
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hb6` (or `8'h39`) and that `y` has the value `4'b1100`. The first row has been filled in as an example.

expression	value
x[3:0]	4'h6 (or 4'h9)
x[7:4]^y	
{ y, x[7:4] }	
x << (y >> 2)	
^x ? 1'b1 : 2'd2	
x + (y >= 9)	

Answers

For `x` having value `8'hb6`:

expression	value
x[3:0]	4'h6
x[7:4] ^ y	4'h7
{ y, x[7:4] }	8'hcb
x << (y >> 2)	8'hb0
^x ? 1'b1 : 2'd2	2'h1
x + (y >= 9)	8'hb7

For `x` having value `8'h39`:

expression	value
x[3:0]	4'h9
x[7:4] ^ y	4'hf
{ y, x[7:4] }	8'hc3
x << (y >> 2)	8'hc8
^x ? 1'b1 : 2'd2	2'h2
x + (y >= 9)	8'h3a

Question 3

A synchronous digital logic circuit operates with a clock rate of 300 MHz. The worst-case propagation delay through any combinational logic path is 2 ns. If the registers in this circuit have a clock-to-output delay of 0.5 ns and a minimum required setup time of 1 ns (or 0.5 ns), will this circuit operate reliably?

Answers

The clock period is $T_{clock} = 1/300\,\text{MHz} = 3.33\,\text{ns}$
   The available setup time is computed as:

$$t_{SU}(\text{avail}) = T_{clock} - t_{CO}(\text{max}) - t_{PD}(\text{max})$$
$$= 3.33 - 0.5 - 2$$
$$= 0.833\,\text{ns}$$

For a required setup time of 1 ns:

$$\text{slack} = t_{SU}(\text{avail}) - t_{SU}(\text{required})$$
$$= 0.833\,\text{ns} - 1\,\text{ns}$$
$$= -0.167\,\text{ns}$$

Since the slack is negative, the circuit may exhibit metastable behaviour and no, the circuit may not operate reliably.
or, for a required setup time of 0.5 ns:

$$\text{slack} = 0.833\,\text{ns} - 0.5\,\text{ns}$$
$$= 0.333\,\text{ns}$$

Since the slack is positive, the circuit should not exhibit metastable behaviour and yes, the circuit should operate reliably.

Question 4

A state machine has two inputs named **a** and **b**, a reset input named **reset**, and a clock input named **clk**. It has *no outputs*. The state transition diagram is shown below. The diagram follows the course guidelines for state transition diagrams.
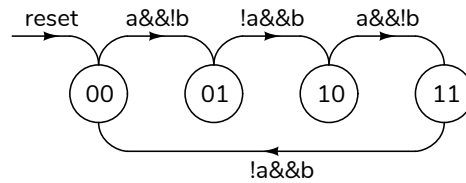
or:
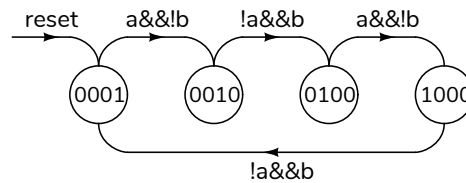
Write a Verilog module named **quad** that implements this state machine. Use the state encodings shown in the diagram. Include the module declaration and any additional required signal declarations. Follow the course coding conventions but omit comments.

Answers

```verilog
module quad
  ( input logic a, b, reset, clk ) ;

  logic [3:0] state ;

  always_ff @(posedge clk)
    state <= reset ? 4'b0001 :
             state == 4'b0001 && a && !b ? 4'b0010 :
             state == 4'b0010 && !a && b ? 4'b0100 :
             state == 4'b0100 && a && !b ? 4'b1000 :
             state == 4'b1000 && !a && b ? 4'b0001 :
             state ;

endmodule
```

or:

```verilog
module quad
  ( input logic a, b, reset, clk ) ;

  logic [1:0] state ;

  always_ff @(posedge clk)
    state <= reset ? 2'b00 :
             state == 2'b00 && a && !b ? 2'b01 :
             state == 2'b01 && !a && b ? 2'b10 :
             state == 2'b10 && a && !b ? 2'b11 :
```

```
                    state == 2'b11 && !a && b ? 2'b00 :
                    state ;
endmodule
```

Question 5

An IC has the following logic level specifications:

Table 5–5. 3.3-V LVTTL Specifications					
Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		−0.5	0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4 mA (1)	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA (1)		0.45	V

(a) What is the noise margin for a high logic level?

(b) What is the noise margin for a low logic level?

Answers

- For the high logic level the noise margin is:
  $V_{OH(min)} - V_{IH(min)} = 2.4 - 1.7 = \boxed{0.7\,\text{V}}$
- For the low logic level the noise margin is:
  $V_{IL(max)} - V_{OL(max)} = 0.8 - 0.45 = \boxed{0.35\,\text{V}}$

Question 6

How many bits of resolution would be needed to obtain a maximum quantization error of $1\,\text{mV}$ for a DAC with an output range of $-1\,\text{V}$ to $1\,\text{V}$?

Answers

If the maximum quantization error is $1\,\text{mV}$ then the difference between quantization levels is twice this, $2\,\text{mV}$.

If the range is $1 - -1 = 2\,\text{V}$, then the minimum numbers of steps is $\log_2(2/0.002) = \log_2(1000) = 9.96$ so $\boxed{10\text{ bits}}$ of resolution are needed.
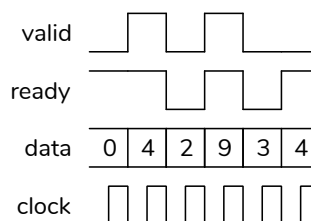
Question 7

A Verilog module has an input declared as `input logic pulse_n`. If the input `pulse_n` is at a low logic level, what is value of the expression: `pulse_n ? 1 : 0`?
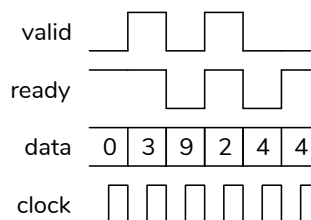
Answers

`pulse_n` is an active-low input. The value of an input is 1 if high and 0 if low. The value of the expression `pulse_n ? 1 : 0` is the same as `1'b0 ? 1 : 0` which is $\boxed{0}$ (or 32'd0).

Question 8

What are the numerical value(s) of the data transferred over a valid/ready interface by the waveforms shown below? Your answer should be a sequence of zero or more numbers that appear in the data waveform.

or:

Answers

Data is transferred when both valid and ready are asserted. This happens when the data has values $\boxed{4, 9}$ (or $\boxed{3, 2}$).

Question 9

When a digital circuit operates at $300\,\text{MHz}$ it consumes $1\,\text{W}$ (or $100\,\text{mW}$). What average power would it consume if it operates half of the time at $300\,\text{MHz}$ and half of the time at $1\,\text{MHz}$?

Answers

The power consumption at a clock frequency of $1\,\text{MHz}$ will be:

$$P_2 = P_1 \cdot \frac{f_2}{f_1}$$
$$= 1\,\text{W} \cdot \frac{1\,\text{MHz}}{300\,\text{MHz}}$$
$$= 3.33\,\text{mW}$$

The average of the power consumption at the two frequencies is $0.5 \times 1\,\text{W} + 0.5 \times 0.003\,33\,\text{W} \approx$ $\boxed{501.7\,\text{mW}}$.

If the power at 300 MHz is 100 mW then the average power will be 10 times less, $\boxed{50.2\,\text{mW}}$.

Question 10

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

ESD	
BGA	
tri-state	
Moore's Law	
ASIC	
NRE	

(1) design cost   (1) design cost

(2) custom IC   (2) IC complexity

(3) open-drain   (3) custom IC

(4) failure cause   (4) failure cause

(5) package   (5) open-drain

(6) IC complexity   (6) package

Answers

ESD	failure cause	4	4
BGA	package	5	6
tri-state	open-drain	3	5
Moore's Law	IC complexity	6	2
ASIC	custom IC	2	3
NRE	design cost	1	1

Note: A tri-state output is different than an open-drain output but both are technologies used to implement bidirectional signals.