ELEX 2117 : Digital Techniques 2
2023 Fall Term

FINAL EXAM
9:00 AM
Friday, December 15, 2023
SW03-1750

This exam has ten (10) questions on three (3) pages. The marks for each question are as indicated. There are a total of thirty-one (31) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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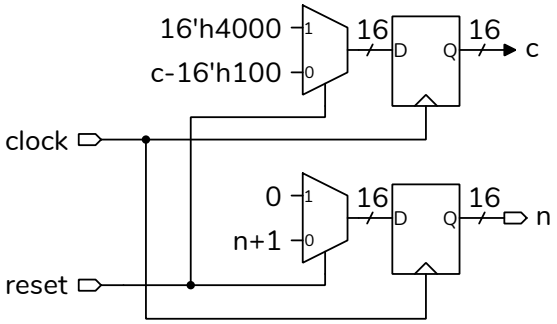
Question 1 — 5 marks

Write a Verilog module corresponding to the schematic shown below. The module name is **`adiv`**. Include the module declaration and any additional required signal declarations. The diagram below follows the course guidelines for schematics. Follow the course coding conventions but omit comments.



Question 2 — 5 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that **`x`** has the value **`8'h39`** and that **`y`** has the value **`4'b1100`**. The first row has been filled in as an example.

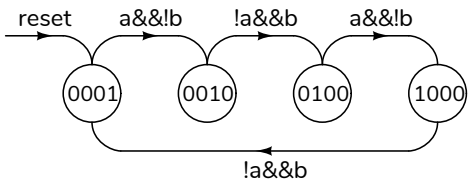
expression	value
`x[3:0]`	`4'h9`
`x[7:4]^y`	
`{ y, x[7:4] }`	
`x << ( y >> 2 )`	
`^x ? 1'b1 : 2'd2`	
`x + ( y >= 9 )`	

Question 3 — 2 marks

A synchronous digital logic circuit operates with a clock rate of 300 MHz. The worst-case propagation delay through any combinational logic path is 2 ns. If the registers in this circuit have a clock-to-output delay of 0.5 ns and a minimum required setup time of 0.5 ns, will this circuit operate reliably?

Question 4 — 4 marks

A state machine has two inputs named **`a`** and **`b`**, a reset input named **`reset`**, and a clock input named **`clk`**. It has *no outputs*. The state transition diagram is shown below. The diagram follows the course guidelines for state transition diagrams.



Write a Verilog module named **`quad`** that implements this state machine. Use the state encodings shown in the diagram. Include the module declaration and any additional required signal declarations. Follow the course coding conventions but omit comments.

Question 5 — 2 marks

An IC has the following logic level specifications:

Table 5–5. 3.3-V LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(1)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(1)*		0.45	V

(a) What is the noise margin for a high logic level?

(b) What is the noise margin for a low logic level?

Question 6 — 2 marks

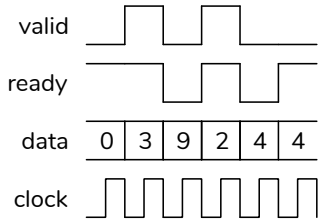
How many bits of resolution would be needed to obtain a maximum quantization error of 1 mV for a DAC with an output range of −1 V to 1 V?

Question 7 — 1 marks

A Verilog module has an input declared as `input logic pulse_n`. If the input `pulse_n` is at a low logic level, what is value of the expression: `pulse_n ? 1 : 0`?

Question 8 — 2 marks

What are the numerical value(s) of the data transferred over a valid/ready interface by the waveforms shown below? Your answer should be a sequence of zero or more numbers that appear in the data waveform.



Question 9 — 2 marks

When a digital circuit operates at 300 MHz it consumes 100 mW. What average power would it consume if it operates half of the time at 300 MHz and half of the time at 1 MHz?

Question 10 — 6 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

ESD	
BGA	
tri-state	
Moore's Law	
ASIC	
NRE	

(1) design cost

(2) IC complexity

(3) custom IC

(4) failure cause

(5) open-drain

(6) package

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Sample Exam 2 A01234567

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Question 1 — 5 marks

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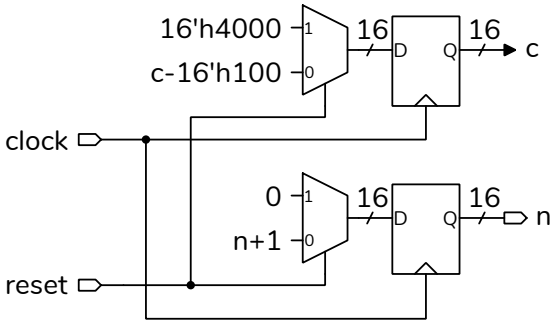

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and that **`x`** has the value **`8'hb6`** and that **`y`** has the value **`4'b1100`**. The first row has been filled in as an example.

expression	value
`x[3:0]`	`4'h6`
`x[7:4]^y`	
`{ y, x[7:4] }`	
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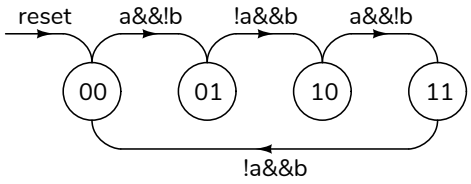

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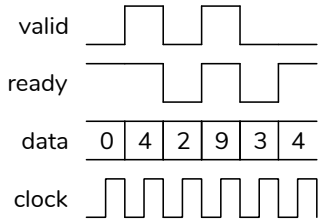

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