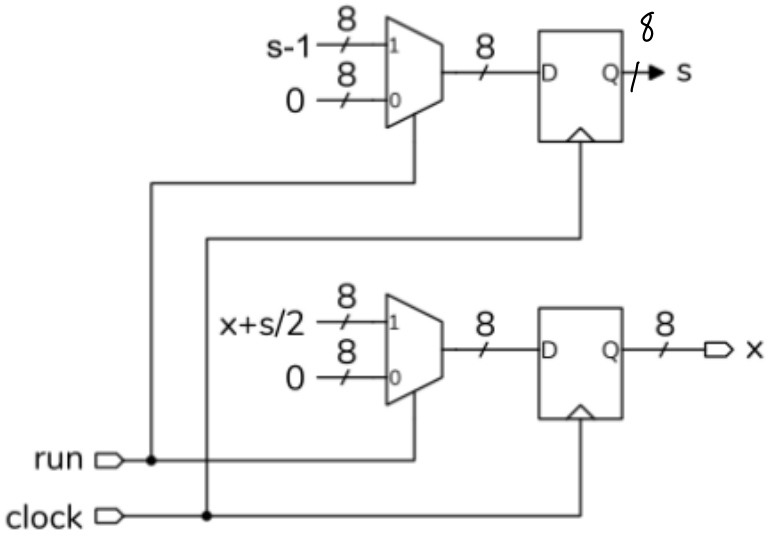
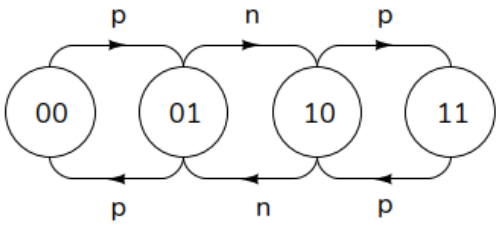



```
module xpos (
    input logic run, clock,
    output logic [7:0] X
    );

logic [7:0] s;

always_ff @(posedge clock)
    S <= run? s-1 : 0;

always_ff @(posedge clock)
    X <= run? x+s/2 : 0 ;

endmodule
```

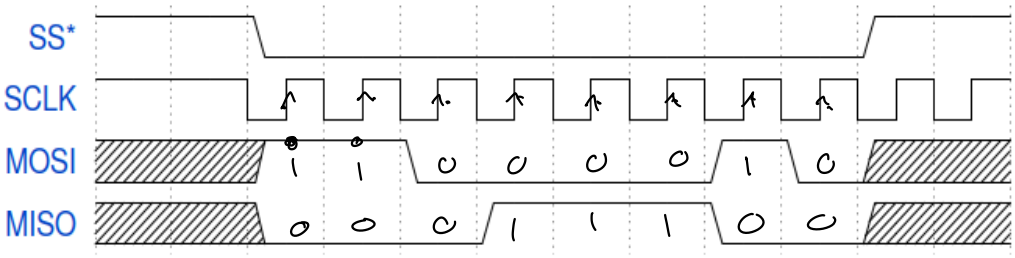
```
logic [7:0] x = 8'hac;
logic [3:0] y = 4'b1001 ;
```

expression	value
{x[3:0],y[3:0],x[7:4]}	12'hc9a
!x&&x	1'h0
~x|x	8'hff
x<<2 + 2'd3	8'h80
y/2	32'h4
x[3:0] > y	1'h1
x^y	8'ha5
x[0] ? x : y	8'h9

signal name	truth value (T/F)	truth value in an expression (0/1)	logic level (H/L)	Verilog value when input (0/1)
$\overline{\text{busy}}$	T	1 T	L	0 → L
dark	F	0 F	L	0 → L
even*	F	0 F	H	1 → H
$\overline{\text{short}}$	T	1 T	L	0 → L




```
always_ff @(posedge clock)
state <= state==2'b00 && p ? 2'b01:
         state==2'b01 && n ? 2'b10:
         state==2'b10 && p ? 2'b11:
         state==2'b11 && p ? 2'b10:
         state==2'b10 && n ? 2'b01:
         state==2'b01 && p ? 2'b00:
         state;
```

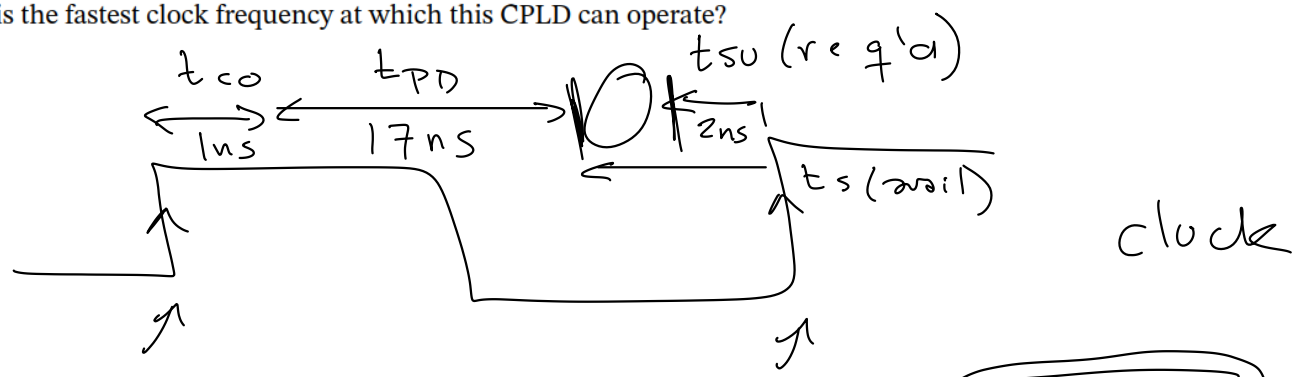


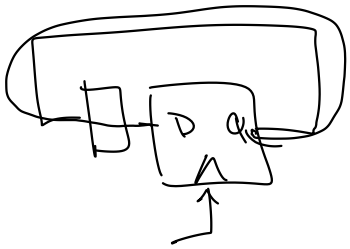
- 8 bits
- master (out) to slave
- master (in) from slave.

master-to-slave: 8'b11000010 = 8'hc2

slave to master: 8'h1c

The maximum propagation delay through any combinational logic path in a CPLD is 17 ns, the minimum setup time of its registers is 2 ns and the maximum clock-to-output delay is 1 ns. What is the fastest clock frequency at which this CPLD can operate?





slack==0 when $t_{su}(avail) = t_{su}(req'd)$.

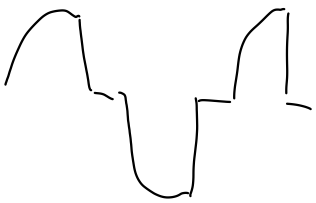
$T_{clock(min)} = 1 + 17 + 2 = 20\,ns$.

$f_{clock(max)} = \frac{1}{20 \times 10^{-9}} = 50\,MHz$

Question 7 — 2 marks

A digital power quality analyzer needs to measure the level of harmonics up to the 50'th harmonic of the 60 Hz power line frequency (i.e. up to 3000 Hz) with a quantization SNR of over 80 dB.

What minimum ADC sampling rate is required? What number of bits of resolution is required?



$f_{samp} > 2 \times f_{max}$

$> 2 \times 3000$

$f_{samp} > 6000\,Hz$

$SNR \approx 1.8 + 6B\,(dB)$ (B = #bits)

> 80

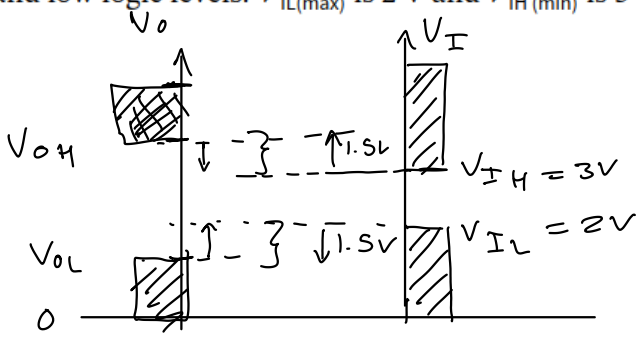
$1.8 + 6B > 80$

$B > \frac{80 - 1.8}{6} = 13.04$

$B = 13$ bits (or 14).

Question 8 — 2 marks

You are choosing the logic levels for a new design and need to maintain a noise margin of 1.5 V for both high and low logic levels. $V_{IL(max)}$ is 2 V and $V_{IH\,(min)}$ is 3 V. What are $V_{OL(max)}$ and $V_{OH(min)}$?



$V_{OH}(min) = V_{IH}(min) + 1.5V$

$= 3 + 1.5$

$\boxed{V_{OH}(min) = 4.5V}$

$V_{OL}(max) = V_{IL}(max) - 1.5V$

$= 2 - 1.5$

$\boxed{V_{OL}(max) = 0.5V}$

Question 9 — 2 marks

A CMOS digital logic circuit operates from a 1.5 V battery for 20 hours before the battery is exhausted. How long would the same battery last if the clock frequency was reduced by a factor of 20? *Hint: Battery life is inversely proportional to current consumption.*

$\frac{P_2}{P_1} = \frac{f_2}{f_1}\left(\frac{V_2}{V_1}\right)^2$ $\quad V_2 = V_2$ $\quad \frac{P_2}{P_1} = \frac{V_2 I_2}{V_1 I_1}$

$\frac{P_2}{P_1} = \frac{I_2}{I_1} = \frac{f_2}{f_1} = \frac{1}{20}$ $\quad \frac{f_2}{f_1} = \frac{1/20}{1}$

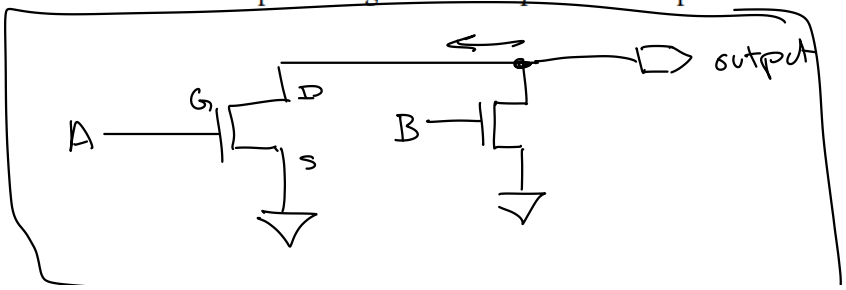
$\frac{I_2}{I_1} = \frac{1}{20}$

$\frac{T_2}{T_1} = \frac{I_1}{I_2}$ (inversely proportional).

$\boxed{T_2 = 20\,T_1}$ battery life increases by 20x.

Question 10 — 1 marks

Draw the schematic of a two-input NOR gate with an *open-drain* output. Use MOSFET transistors.



Question 11 — 5 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

fabless	1
die	2
TQFP	4
wafer	5
CPLD	3

(1) manufacturer

(2) chip

(3) programmable

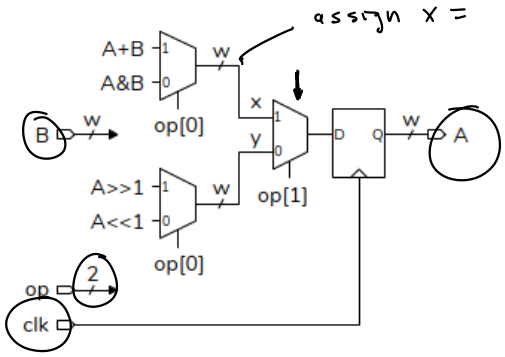
(4) package

(5) 300 mm

Write a Verilog module named **alu** corresponding to the diagram shown below. The module has a w-bit input **B**, a 2-bit input **op**, a clock input **clk**, and a **w**-bit registered output **A**. The module declaration should include a parameter named **w** for the bus widths with a default value of 16. The use of the signals **x** and **y** is optional but they must be declared if they're used. Bits should be numbered in decreasing order. Follow the course coding conventions. You may omit comments.

op [1]
op [0]

op[1]
op[0]



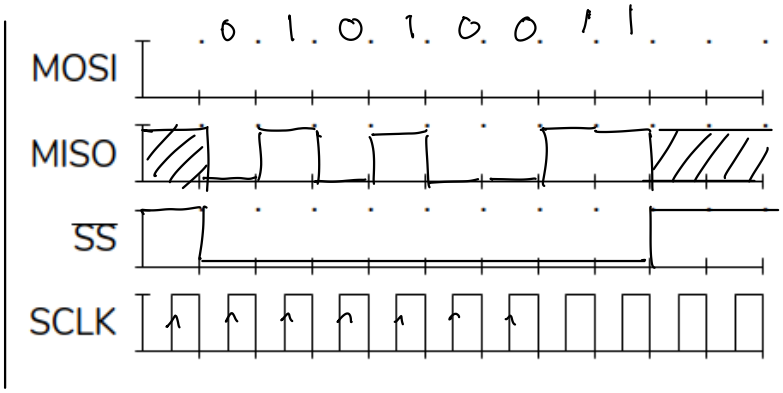

```
module alu #(parameter w=16)
  (input logic [w-1:0] B,
   input logic [1:0] op,
   input logic clk,
   output logic [w-1:0] A);

logic [w-1:0]x,y;

always_ff @(posedge clk)
    A <= op[1]? x : y;

assign x = op[0] ? A+B : A&B;

assign y = op[0] ? A>>1 : A<<1;

endmodule
```

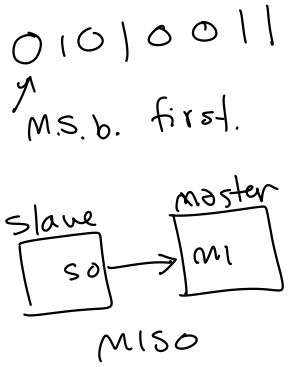
```
logic [7:0] x = 8'h5a ;
logic [3:0] y = 4'b0011 ;
```

expression	value
{x[3:0],x[7:4]}	
!x||x	
~x|x	
x >> 1 + 1'b1	
2*y	
x[1:0] > y	
x^y	
!y ? x : x^y	

Question 3 — 5 marks

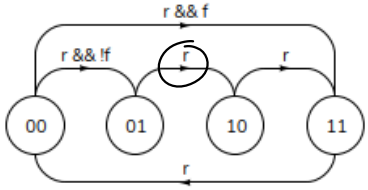
Draw the waveforms that would be used to transfer a byte that has the value `8'h53` (in Verilog notation) from the slave to the master over an SPI interface. Draw the waveforms for $\overline{\texttt{SS}}$, and the appropriate data signal (either `MOSI` or `MISO`, but not both). Follow the conventions shown in the lecture notes, including the timing of $\overline{\texttt{SS}}$ relative to the data, the data relative to `SCLK`, and that the most significant bit is transferred first.





Write the state transition table for a state machine that has the following state transition diagram. The state machine has two one-bit inputs: `r` and `f`. The value in each circle is the 2-bit binary encoding of that state. The Verilog expression above a state transition defines the condition for a transition between the two states. Conditions that do not result in a change of state are not shown.

Include columns for the current state, the `r` and `f` inputs, and the next state. You may use the conventions described in the lecture notes including `x` for "don't-care." You need not include input conditions that do not result in a change of state.



current state	inputs r	inputs f	next state
00	1	0	01 -
00	1	1	11 -
01	1	X	10 -
10	1	X	11 -
11	1	X	00 -
S	X	X	S ←

r && !f

r=1 f=0