Solutions to Quiz 3

There were two versions of the first three questions. The values and the answers for the two versions are given below.

Question 1

A flip-flop has an (asynchronous) reset input. The data sheet specifies a minimum time from this input being asserted (or de-asserted) to the output going to zero (or the next rising edge on the clock input). Is this timing specification a guaranteed response or a requirement? How do you know?

Answers

There were two different answers:

- A timing specifications measured to a transition on an output is a guaranteed response.
- A timing specifications measured to a transition on an input, such as the clock, is a requirement.

Question 2

A circuit operating at a clock rate of 50 (or 25) MHz uses registers with a 5 ns setup time and a 1 ns clock-to-output delay. What is the maximum allowable propagation delay through any combinational logic path?

Answers

The equation:

$$t_{SU}\text{ (avail)} = T_{clock} - t_{CO}\text{ (max)} - t_{PD}\text{ (max)}$$

can be solved for t_{PD}:

$$t_{PD}\text{ (max)} = T_{clock} - t_{CO}\text{ (max)} - t_{SU}\text{ (avail)} \quad .$$

For this question $T_{clock} = 1/50\,\text{MHz} = 20\,\text{ns}$ (or 40 ns), t_{CO} is given as 1 ns and t_{SU} as 5 ns. Thus t_{PD} (max) = 20−1−5 = 14 ns. (or t_{PD}(max) = 40−1−5 = 34 ns).

Question 3

A prototype of a circuit consumes 1 (or 2) W when operating with a 5 V supply at a frequency of 5 MHz. What clock rate would reduce the power consumption to 30 mW at a supply voltage of 1.5 V?

Answers

Solving the equation:

$$\frac{P_2}{P_1} = \frac{f_2}{f_1} \cdot \left(\frac{V_2}{V_1}\right)^2$$

for f_2:

$$f_2 = \frac{f_1 P_2}{P_1}\left(\frac{V_1}{V_2}\right)^2$$

and setting $f_1 = 5\times10^6$, $P_1 = 1$ (or 2), $P_2 = 30\times10^{-3}$, $V_1 = 5$ and $V_2 = 1.5$:

$$f_2 = \frac{5\times10^6 30\times10^{-3}}{1}\left(\frac{5}{1.5}\right)^2 = \boxed{1.66\,\text{MHz}}$$

(or 0.833 MHz).

Question 4

Would an open-collector output with a 10 kΩ pull-up resistor operate properly at a frequency of 10 MHz if the parasitic capacitances connected to this output totalled 20 pF? Why or why not? *Hint: What is the time constant?*

Answers

The rise-time time constant is given by $RC = 10\,\text{k}\Omega \times 20\,\text{pF} = 200\,\text{ns}$ while the clock period is $1/10\,\text{MHz} = 100\,\text{ns}$. Thus the signal will need 200 ns to switch between a zero output voltage and ≈ 63% of the high output voltage. This delay exceeds the clock period and such a circuit is unlikely to operate properly.