ELEX 2117 : Digital Techniques 2
2022 Fall Term

Quiz 3
9:30 – 10:20
Friday, November 18, 2022
SW01-1025

This exam has four (4) questions on one (1) pages. The marks for each question are as indicated. There are a total of seven (7) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 1 marks

A flip-flop has an (asynchronous) reset input. The data sheet specifies a minimum time from this input being de-asserted to the next rising edge on the clock input. Is this timing specification a guaranteed response or a requirement? How do you know?

Question 2 — 2 marks

A circuit operating at a clock rate of 25 MHz uses registers with a 5 ns setup time and a 1 ns clock-to-output delay. What is the maximum allowable propagation delay through any combinational logic path?

Question 3 — 2 marks

A prototype of a circuit consumes 2 W when operating with a 5 V supply at a frequency of 5 MHz. What clock rate would reduce the power consumption to 30 mW at a supply voltage of 1.5 V?

Question 4 — 2 marks

Would an open-collector output with a 10 kΩ pull-up resistor operate properly at a frequency of 10 MHz if the parasitic capacitances connected to this output totalled 20 pF? Why or why not? *Hint: What is the time constant?*

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Paper, Test 2 A00123456

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Name: _____

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Question 1 — 1 marks

A flip-flop has an (asynchronous) reset input. The data sheet specifies a minimum time from this input being asserted to the output going to zero. Is this timing specification a guaranteed response or a requirement? How do you know?

Question 2 — 2 marks

A circuit operating at a clock rate of 50 MHz uses registers with a 5 ns setup time and a 1 ns clock-to-output delay. What is the maximum allowable propagation delay through any combinational logic path?

Question 3 — 2 marks

A prototype of a circuit consumes 1 W when operating with a 5 V supply at a frequency of 5 MHz. What clock rate would reduce the power consumption to 30 mW at a supply voltage of 1.5 V?

Question 4 — 2 marks

Would an open-collector output with a 10 kΩ pull-up resistor operate properly at a frequency of 10 MHz if the parasitic capacitances connected to this output totalled 20 pF? Why or why not? *Hint: What is the time constant?*