ELEX 2117 : Digital Techniques 2
2022 Fall Term

Quiz 2
9:30 – 10:00
Friday, October 21, 2022
SW01-1025

This exam has two (2) questions on one (1) pages. The marks for each question are as indicated. There are a total of seven (7) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

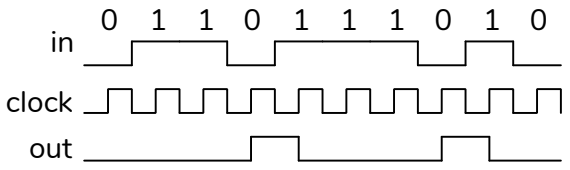
Signature: _____

Question 1 — 5 marks

A state machine detects sequences on a one-bit input named **`in`**. These sequences consist of a **`0`**, followed by two or three **`1`**'s, followed by one **`0`**. The inputs are present on **`in`** on the rising edge of a clock.

An output named **`out`** should be set to **`1`** for one clock period when one of these sequences is detected. Otherwise **`out`** should be set to **`0`**.

An example of the **`in`**, **`clock`** and **`out`** waveforms is shown at right:



(a) What is the maximum length (in bits) of these sequences?

(b) What is the minimum length (in bits) of these sequences?

(c) Draw the state transition diagram. Label each state transition with the required value(s) of **`in`**. *Hint: Use the number of values detected in the sequence, including zero, and a 'detected' state as the states.*

(d) For which state(s) is the value of **`out`** equal to **`1`**?

Question 2 — 2 marks

An input to a Verilog module is named **`hot`**. The current value of **`hot`** indicates that something is currently hot (true).

(a) Is this input currently high or low?

(b) What is the value of the Verilog expression **`!hot`**?

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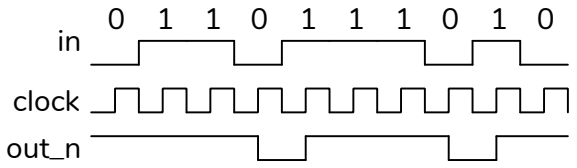
An output named **`out_n`** should be set to **`0`** for one clock period when one of these sequences is detected. Otherwise **`out_n`** should be set to **`1`**.

An example of the **`in`**, **`clock`** and **`out_n`** waveforms is shown at right:



(a) What is the maximum length (in bits) of these sequences?

(b) What is the minimum length (in bits) of these sequences?

(c) Draw the state transition diagram. Label each state transition with the required value(s) of **`in`**. *Hint: Use the number of values detected in the sequence, including zero, and a 'detected' state as the states.*

(d) For which state(s) is the value of **`out_n`** equal to **`0`**?

Question 2 — 2 marks

An input to a Verilog module is named **`hot_n`**. The current value of **`hot_n`** indicates that something is currently hot (true).

(a) Is this input currently high or low?

(b) What is the value of the Verilog expression **`!hot_n`**?