Solutions to Quiz 1

There were two versions of each question. The values and the answers for the two versions are given below.

Question 1

Write a Verilog module named **foo** with a 3 (or 4)-bit input named **x** (or **a**) and 1 (or 2)-bit output named **y**. The module should be empty except for an **endmodule**.

Answers

```
module foo ( input logic [2:0] x,
             output logic y ) ;
endmodule
```

```
module foo2 ( input logic [3:0] a,
              output logic [1:0] y ) ;
endmodule
```

Question 2

Write a Verilog numeric literal that has a value of 33 (decimal), a length of 12 (or 10) bits, and whose value is specified using hexadecimal (or binary) base.

Answers

12'h21 or **10'b10_0001**.

Question 3

Fill in the table on the right with the value of the each expression as a Verilog numeric literal including the correct length and value in hexadecimal base assuming the following declarations:

```
logic [11:0] x;
logic [3:0] y;
```

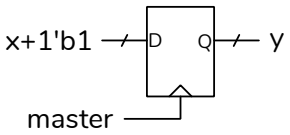
and that **x** has the value **12'h0b5** (or **12'h05b**) and that **y** has the value **4'b1001** (or **4'b0110**).

expression	12'hb5, 4'b1001	12'h5b, 4'b0110
x>>4	12'hb	12'h5
x[7:4]	4'hb	4'h5
{x,y}	16'hb59	16'h5b6
x & y	12'h1	12'h2
x - y	12'hac	12'h55
x[0] ? y : ~y	4'h9	4'h6

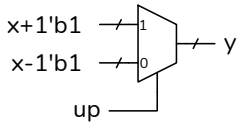
Question 4

Write *one* Verilog statement that implements the block diagram on the right. The buses have been declared as **logic** arrays.

Answers




```
always_ff @(posedge master) y <= x + 1'b1 ;
```



.

```
assign y = up ? x + 1'b1 : x - 1'b1 ;
```