

ELEX 2117 : Digital Techniques 2
2022 Fall Term

Quiz 1

9:30 – 10:00

Friday, September 23, 2022

SW01-1025

This exam has four (4) questions on one (1) pages. The marks for each question are as indicated. There are a total of fifteen (15) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1

3 marks

Write a Verilog module named `foo` with a 4-bit input named `a` and 2-bit output named `y`. The module should be empty except for an `endmodule`.

Question 2

3 marks

Write a Verilog numeric literal that has a value of 33 (decimal), a length of 10 bits, and whose value is specified using binary base.

Question 3

5 marks

Fill in the table on the right with the value of the each expression as a Verilog numeric literal including the correct length and value in hexadecimal base assuming the following declarations:

```
logic [11:0] x;
```

```
logic [3:0] y;
```

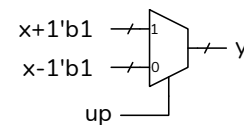
and that `x` has the value `12'h05b` and that `y` has the value `4'b0110`.

expression	value
<code>x>>4</code>	12'hb 12'h5
<code>x[7:4]</code>	
<code>{x,y}</code>	
<code>x & y</code>	
<code>x - y</code>	
<code>x[0] ? y : ~y</code>	

Question 4

4 marks

Write *one* Verilog statement that implements the block diagram on the right. The buses have been declared as `logic` arrays.



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Paper, Test 2 A00123456

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Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1

3 marks

Write a Verilog module named `foo` with a 3-bit input named `x` and 1-bit output named `y`. The module should be empty except for an `endmodule`.

Question 2

3 marks

Write a Verilog numeric literal that has a value of 33 (decimal), a length of 12 bits, and whose value is specified using hexadecimal base.

Question 3

5 marks

Fill in the table on the right with the value of the each expression as a Verilog numeric literal including the correct length and value in hexadecimal base assuming the following declarations:

```
logic [11:0] x;
```

```
logic [3:0] y;
```

and that `x` has the value `12'h0b5` and that `y` has the value `4'b1001`.

expression	value
<code>x>>4</code>	<code>12'hb</code>
<code>x[7:4]</code>	
<code>{x,y}</code>	
<code>x & y</code>	
<code>x - y</code>	
<code>x[0] ? y : ~y</code>	

Question 4

4 marks

Write *one* Verilog statement that implements the block diagram on the right. The buses have been declared as `logic` arrays.

