ELEX 2117 : Digital Techniques 2
2022 Fall Term

MIDTERM EXAM 1
15:30 – 17:20
Friday, October 7, 2022
SW03-1710

This exam has five (5) questions on two (2) pages. The marks for each question are as indicated. There are a total of sixteen (16) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 2 marks

Define a Verilog lookup table named **`double`** that can be used to determine double the value of a number between 0 and 7. The result should be a 6-bit value between between 0 and 14. For example, the expression **`double[5]`** should have the value **`6'd10`**. Write only the lookup table definition, not a complete module.

Question 2 — 2 marks

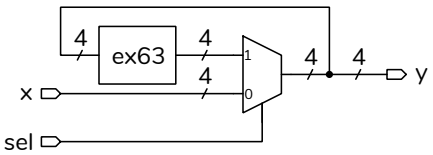
What minimum size of counter is needed to implement a timer that has a duration of 20 ms using a 2.5 MHz clock? Your answer should be the number of bits. Show your work.
If this timer's counter counts down to zero, what range of values will the counter take on?

Question 3 — 4 marks

Write a Verilog module named **`ymod`** corresponding to the block diagram below. The block labelled **`ex63`** represents a module named **`ex63`** defined as:

```
module ex63
  ( input  logic [3:0] a,
    output logic [3:0] b ) ;
   //...
endmodule
```

Write only the module **`ymod`**. The module inputs and outputs should be as shown in the diagram. The module should include definitions for any additional signal(s) required to instantiate the **`ex63`** module.



Question 4 — 4 marks

A state machine has a an input named **`rst`**, a clock input named **`clk`** and an output named **`s`**. **`s`** can take on the values **`000`**, **`001`**, **`011`**, and **`111`**. The state machine operates as follows:

- If **`rst`** is asserted (has the value 1) then **`s`** is set to **`111`**.
- If **`rst`** is not asserted then **`s`** takes on the values **`011`**, **`001`**, and **`000`**, in that order, and then stays at the value **`000`** until **`rst`** is asserted again.

Write a state transition table for this state machine. Include columns for the current state, the **`rst`** input and the next state.

Question 5 — 4 marks

Below is the Verilog code for a state machine. Draw the state transition diagram. Label all states. Label all transition conditions using Verilog expressions.

```
module blink
  ( input  logic clock, reset,
    output logic [3:0] leds ) ;

   always_ff @(posedge clock)
     leds <= reset ? 4'b1111 :
             leds == 4'b1111 ? 4'b0011 :
             leds == 4'b0011 ? 4'b0001 :
             leds == 4'b0001 ? 4'b0000 : leds ;

endmodule
```

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This exam paper is for:

Sample Exam 2 A01234567

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Name: _____

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Question 1 — 2 marks

Define a Verilog lookup table named **square** that can be used to determine the square of a number between 0 and 7. The result should be a 6-bit value between between 0 and 49. For example, the expression **square[5]** should have the value **6'd25**. Write only the lookup table definition, not a complete module.

Question 2 — 2 marks

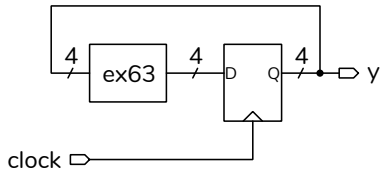
What minimum size of counter is needed to implement a timer that has a duration of 10 ms using a 2.5 MHz clock? Your answer should be the number of bits. Show your work.
If this timer's counter counts down to zero, what range of values will the counter take on?

Question 3 — 4 marks

Write a Verilog module named **ymod** corresponding to the block diagram below. The block labelled **ex63** represents a module named **ex63** defined as:

```
module ex63
  ( input  logic [3:0] a,
    output logic [3:0] b ) ;
   //...
endmodule
```

Write only the module **ymod**. The module inputs and outputs should be as shown in the diagram. The module should include definitions for any additional signal(s) required to instantiate the **ex63** module.



Question 4 — 4 marks

A state machine has a an input named **rst**, a clock input named **clk** and an output named **s**. **s** can take on the values **000**, **001**, **011**, and **111**. The state machine operates as follows:

- If **rst** is asserted (has the value 1) then **s** is set to **000**.
- If **rst** is not asserted then **s** takes on the values **001**, **011**, and **111**, in that order, and then stays at the value **111** until **rst** is asserted again.

Write a state transition table for this state machine. Include columns for the current state, the **rst** input and the next state.

Question 5 — 4 marks

Below is the Verilog code for a state machine. Draw the state transition diagram. Label all states. Label all transition conditions using Verilog expressions.

```
module blink
  ( input  logic clock, reset,
    output logic [3:0] leds ) ;

   always_ff @(posedge clock)
     leds <= reset ? 4'b1000 :
             leds == 4'b1000 ? 4'b1100 :
             leds == 4'b1100 ? 4'b1110 :
             leds == 4'b1110 ? 4'b1111 : leds ;

endmodule
```