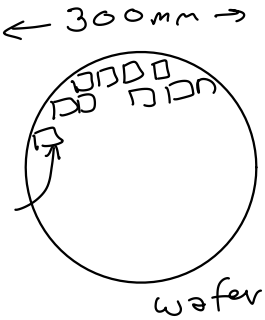
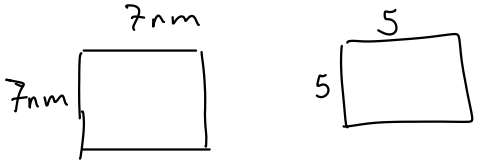
Programmable Logic Applications and Architectures

Exercise 1: What improvement in number of transistors per unit area would be achieved by reducing the transistor dimensions from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?

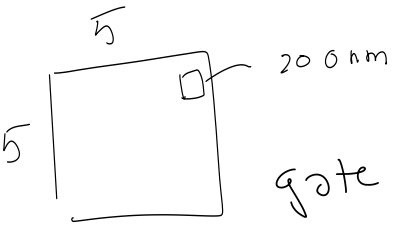




$49\ nm^2 \rightarrow 25\ nm^2$ reduced area to $\frac{25}{49} \approx 50\%$

$$\pi\left(\frac{300}{2}\right)^2 mm = \frac{70{,}000\ mm^2}{5 \times 5\ mm^2} \approx 3000\ \text{die}$$

πr^2



gate area $= (0.2 \times 10^{-6})^2$

die area $= (5 \times 10^{-3})^2$

$$\#\ \text{gates} = \frac{25 \times 10^{-6}}{.04 \times 10^{-12}} = 6.25 \times 10^6\ \text{gates}$$

Exercise 2: Would you use hardware or software to implement: A calculator? A controller for kitchen appliance? An Ethernet interface? To do Cryptocurrency "mining"?

	operations	time allowed	ops/second	can do in software?
microwave oven	100	1 s.	100	Y
calculator	1000	0.1 s.	10,000.	Y
ethernet i/f 1 Gb/s	10	1×10^{-9} s	10^{10}	N
"mining"	→	→	→	N

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?