Analog Interfaces

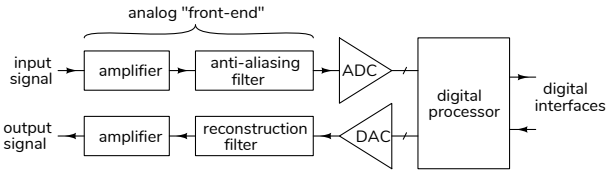
A Digital-to-Analog converter (DAC or D/A) converts discrete ("digital") signals to continuous ("analog") ones. A Digital-to-Analog converter (ADC or A/D) does the reverse. This lecture describes their specifications and some common implementations.
After this lecture you should be able to solve problems involving: sampling rate vs signal frequencies; number of bits vs resolution and quantization SNR; clock rate, sample rate and resolution for binary-weighted DAC, PWM DAC, flash ADC, SAR ADC and clock rates, sample rate and resolution; compare

Introduction

Signals are time-varying voltages or currents. Analog signals are continuous in time and voltage. Examples include the voltages produced by microphones and image sensors, the outputs of strain gauges that measure forces,the currents that control electric motors, the radio-frequency signals on to an antenna for wireless communication, and many others.

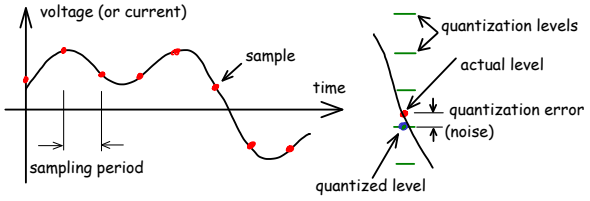
In most cases these analog signals are converted to or from a digital form for processing. This is because processing digital representations of these signals is less expensive, consumes less power and is more precise than processing signals in their analog form.

The diagram below shows the various functions involved in processing analog signals in digital form. These will be described in this lecture.



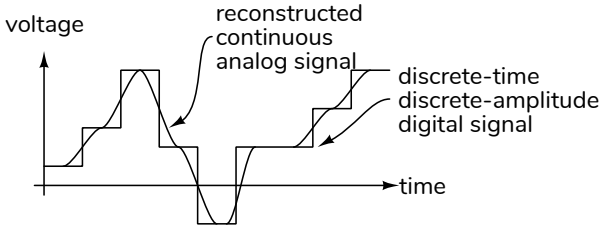
Sampled Waveforms

To represent signals in digital form, the analog signal is sampled (measured) at a regular rate called the "sampling rate." Each sample is then converted into a binary number with a fixed number of bits. Thus the signal becomes discrete in both time and voltage. The circuit that does this is called an analog-to-digital converter (ADC or A/D).



A digitized signal can be converted to a continous signal by generating a step-like waveform with the required levels at the required sampling rate. The circuit that does this is called a digital-to-analog converter (DAC or D/A).

This waveform is then smoothed into a continous signal by low-pass filtering with a "reconstruction" filter.



Sampling Rate and Resolution

The two most important specifications for digitized signals are the sampling rate and the resolution.

The sampling rate (or frequency) must be high enough to be able to accurately reconstruct the original signal. The Nyquist sampling theorem states that a signal can be exactly reconstructed if it is sampled at more than twice the highest frequency of the signal. If the sampling rate is too low then frequency components will be "aliased" and appear at a different, lower frequency. To avoid this, the analog signal can be low-pass filtered with an "anti-aliasing" filter to remove frequency components above half of the sampling rate.

Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one that demonstrates aliasing and one that does not. Is it sufficient to sample at twice the highest frequency of the analog signal?

Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to include frequency components up to the 7'th harmonic (at 70 kHz)?

Digitized signals are represented as n-bit binary numbers where each of the 2^n possible values represents a different voltage. If the range of voltage levels that can be quantized is V then the difference between each quantized voltage level is $\Delta = {}^{V}/_{(2^n-1)}$.

Exercise 3: A signal with range of ± 3 V must be quantized so that the quantization error is less than 1 mV. What minimum number of bits of resolution is required?

Quantizing a signal requires that the signal be rounded off to the nearest quantized voltage level. This is equivalent to adding "quantization noise." For some applications the ratio of signal power to the power of this quantization noise is a useful specification. This quantization signal-to-noise ratio (SNR) for a full-scale sine wave input is $1.76 + 6n$ dB[1]. If the quantization SNR is known then this equation can be solved for the effective number of bits (ENOB), n.

Exercise 4: A signal-to-noise power ratio of about 48 dB is considered good enough for speech communication. Approximately how many bits per sample are required to obtain this quantization SNR?

Exercise 5: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

Other specifications that are important for specific applications include:

monotonic Each increase in digital value also results in an increase of the analog value.

linearity The maximum deviation from an ideal straight-line relationship between digital and analog values

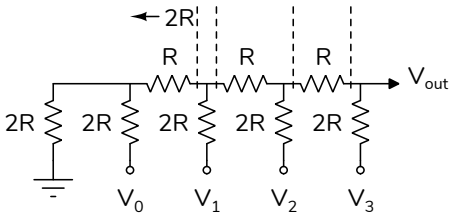
distortion There are several ways of measuring distortion, often in terms of the frequency components generated by the distortion.

[1] For other waveforms the value depends on the type of signal being digitized.

Digital-to-Analog Converters

Binary Weighted DAC

We can use each bit of the quantized signal to control the addition of binary-weighted voltages to the output. The most-significant bit controls adding a value of $V_{\text{ref}}/2$, the next-most-significant bit controls adding a value of $V_{\text{ref}}/4$ and so on. Typical implementations use two resistor values in an "R-2R" voltage divider network. A 4-bit example is:



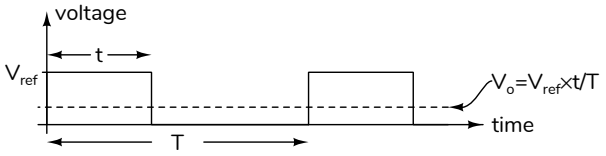
$$V_{\text{out}} = \left(\frac{V_3}{2} + \frac{V_2}{4} + \frac{V_1}{8} + \frac{V_0}{16}\right)$$

where V_i is either V_{ref} or 0.

Exercise 6: Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenim resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{\text{ref}}$).

Pulse Width Modulation

A PWM DAC generates a binary rectangular waveform with a duty cycle ${}^{t}/_{T}$:



When this waveform is low-pass filtered so that only the DC (zero-frequency) component remains, the output is a voltage proportional to the high level voltage (V_{ref}) and the duty cycle.

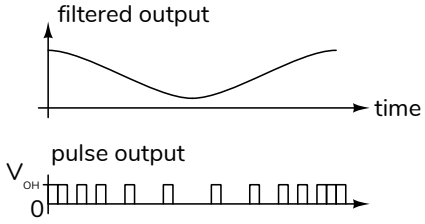
The resolution of a PWM DAC is determined by the number of possible pulse widths. If each pulse is divided into $2^n - 1$ intervals then there are 2^n possible pulse widths.

Exercise 7: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?

Exercise 8: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?

Sigma-Delta DAC

Instead of varying the duty cycle of a constant-period pulse waveform as in PWM, we can vary the frequency at which short, fixed-duration pulses are output. A pulse output increases the output voltage, no output decreases it. The output will be proportional to the average fraction of pulses per time interval. This is called pulse density modulation.



A Sigma-Delta[2] DAC keeps a running (digital) sum of the pulses (positive or negative) and compares the sum to the desired output voltage. A pulse is output whenever the computed output is smaller than the desired output.

Exercise 9: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

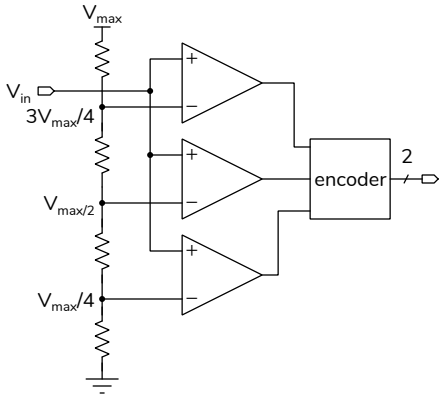
Analog to Digital Converters

Comparators and Flash ADC

The simplest analog to digital converter is a comparator, a circuit that compares two analog inputs and asserts an output when one of the inputs is higher than the other.

An n-bit "flash" ADC can be constructed using $2^n - 1$ reference voltages (thresholds), $2^n - 1$ comparators and priority encoder. The schematic below shows how a voltage range from 0 to $V_{\max}$ can be divided up into four voltage ranges of $V_{\max}/4$ and three comparators can determine which range the input voltage voltage falls into. The priority encoder then converts the three comparator outputs (which can be 000, 001, 011 or 111) into a 2-bit binary output.

[2]It's called Sigma-Delta because we Σ (add) Δ's (increments). Also known as Delta-Sigma.



This is the fastest type of ADC – the sampling rate is equal to the clock rate – but is the most expensive as the complexity increases exponentially with n.

Exercise 10: Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

SAR ADC

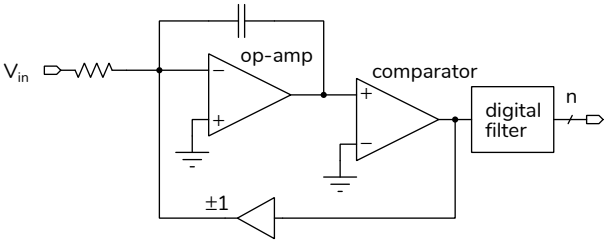
A Successive Approximation Register (SAR) DAC uses a state machine to progressively test the input voltage against thresholds output by a DAC. Instead of a ramp, the threshold voltages are determined by a state machine that does a binary search for the n-bit DAC output that is just smaller than the input voltage.

A SAR ADC can do one conversion per n clock cycles and its complexity increases linearly with n.

Exercise 11: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output?

Sigma-Delta ADC

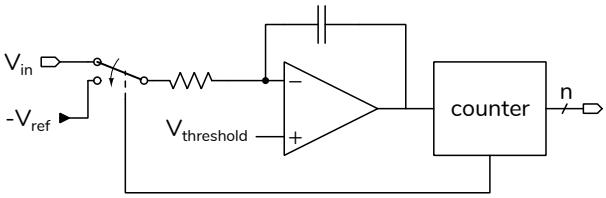
A Sigma-Delta ADC, shown below, integrates the input voltage plus a feedback pulse signal. The polarity of the feedback pulses forces the integrator output to zero.

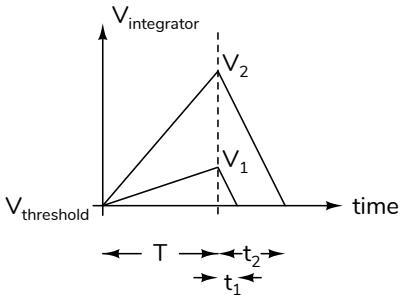


A digital filter measures the fraction of time that the pulse signal is high; this is proportional to the input voltage and is the ADC output.

A Sigma-Delta ADC requires clock rates much higher than (e.g. 100 times)[3] the sampling rate but is inexpensive because it does not require accurate analog components (e.g. the accurate resistors in an R-2R DAC as would be used in a typical SAR ADC).

Dual-Slope ADC





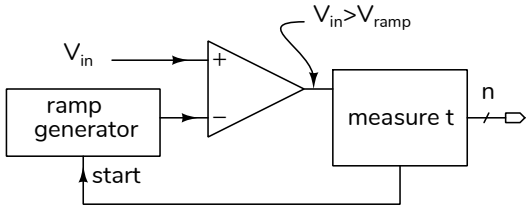
A dual-slope ADC integrates the input for a fixed duration (T) and measures the time required to integrate a negative reference voltage until the integrator is discharged. The ratio t/T is the ratio of V_{in}/V_{ref}. This approach eliminates the dependence on several analog components (integrator R and C, comparator thresholds, and clock rates).

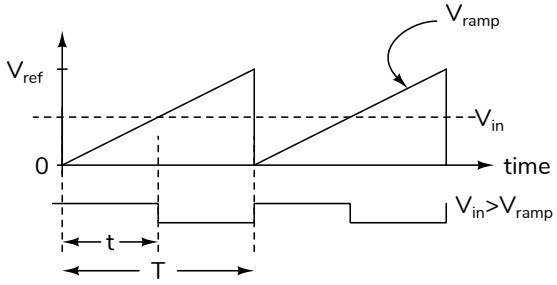
A dual-slope ADC is slow but inexpensive and potentially accurate. It is commonly used in instrumentation.

Exercise 12: What is the slope of an integrator, in V/s, when charging a 100 nF capacitor with 5 V through a 100 kΩ resistor?

Ramp ADC

The ramp ADC uses a comparator to compare the input voltage to a sawtooth (multiple ramp) threshold voltage waveform:





The sawtooth can be generated by an analog circuit (an integrator) or a DAC. The rising edge of the comparator output indicates when the threshold voltage matches the input voltage. The threshold voltage at that point can be determined by measuring the time from the start of the ramp or from the value of the DAC output.

The ramp ADC is simple but when the ramp is implemented with a DAC it is slower than a SAR DAC and when implemented with an integrator it is less accurate than a dual-slope ADC.

Exercise 13: Rank the different ADCs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

[3] The required oversampling ratio, the ratio of clock rate to sampling rate, depends on the desired ENOB and sigma-delta architecture.