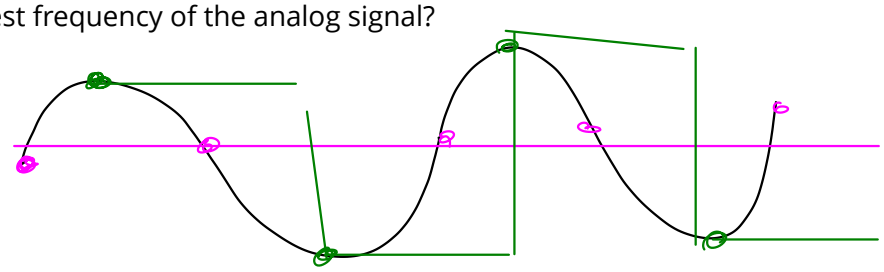
Analog Interfaces

Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one that demonstrates aliasing and one that does not. Is it sufficient to sample at twice the highest frequency of the analog signal?



0 – $\frac{f_s}{2}$

no, must sample at $> 2 \times f_{max}$.

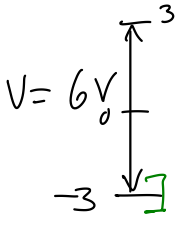
Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to include frequency components up to the 7'th harmonic (at 70 kHz)?

$f_{sample} > 2 \times f_{max}$ ← Nyquist

$> 2 \cdot 70\ kHz$

$> 140\ kHz$

Exercise 3: A signal with range of ±3 V must be quantized so that the quantization error is less than 1 mV. What minimum number of bits of resolution is required?



$\Delta = 0.001$ $\quad \frac{V}{2^n - 1} = \Delta$

$n = log_2\left(\frac{V}{\Delta}\right) = log_2 \frac{6}{.001} = log_2\ 6000 - 1 = 12.55$

need to round up to $n = \underline{13}$ bits

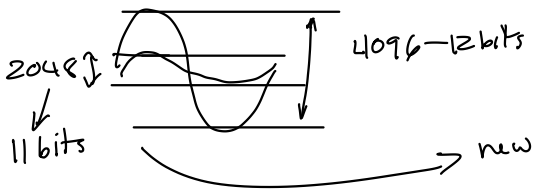
Exercise 4: A signal-to-noise power ratio of about 48 dB is considered good enough for speech communication. Approximately how many bits per sample are required to obtain this quantization SNR?

$$2 + 6n = 48$$

$$n = \frac{48-2}{6} \simeq 7. \rightarrow \text{round up to } n = 8 \text{ bits}$$

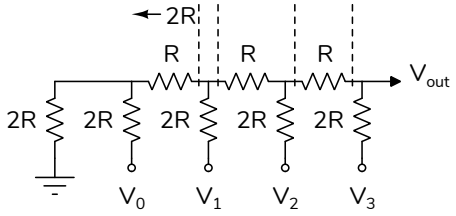
Exercise 5: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

12 bits → $2 + 6 \cdot 12 = 74$ dB SNR

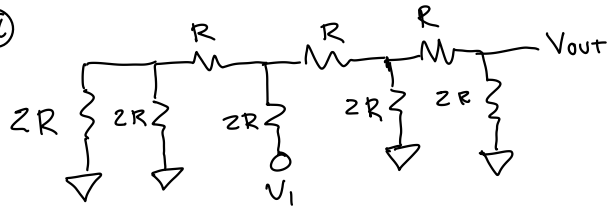


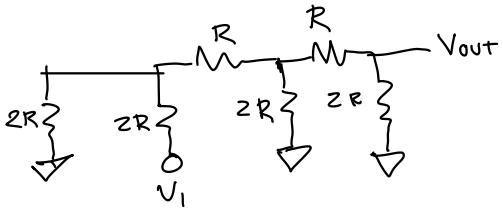
SNR = $2 + 6 \cdot 11 = 68$

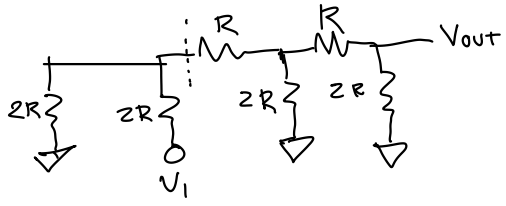
Exercise 6:

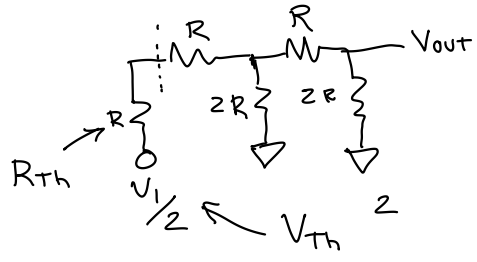


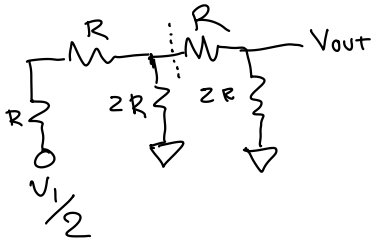
Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenim resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{ref}$).

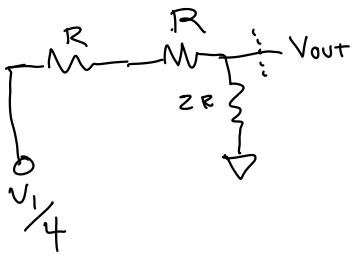
① 

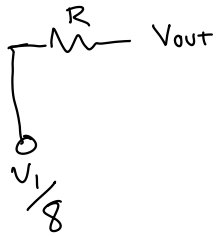
② 

③ 

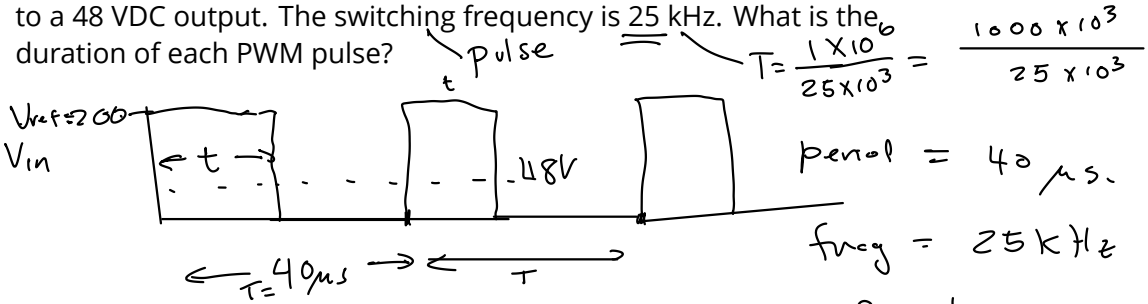
④ 

⑤ 

⑥ 

⑦ 

Exercise 7: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?



$$V_o = \frac{t}{T} \cdot V_{ref}$$

$$t = \frac{V_o}{V_{ref}} T = \frac{48}{200} \cdot 40\mu s. \approx 10\ \mu s.$$

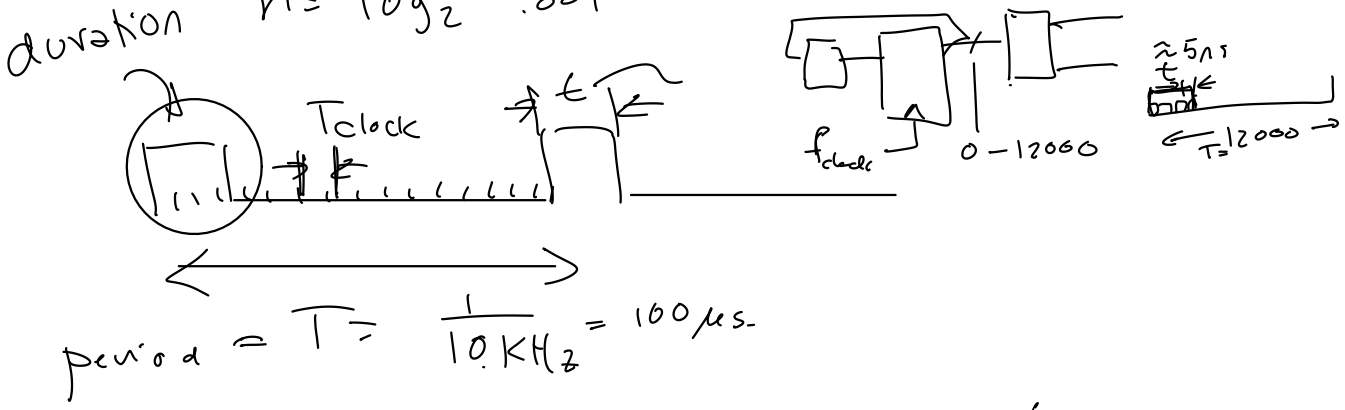
Exercise 8: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?

V=12
Δ=0.001
n=?

$$\Delta = \frac{V}{2^n}$$

$$2^n = \frac{V}{\Delta}, \quad \log_2 2^n = n = \log_2 \frac{V}{\Delta}$$

$$n = \log_2 \frac{12}{.001} = 14 \text{ bits (round up).}$$



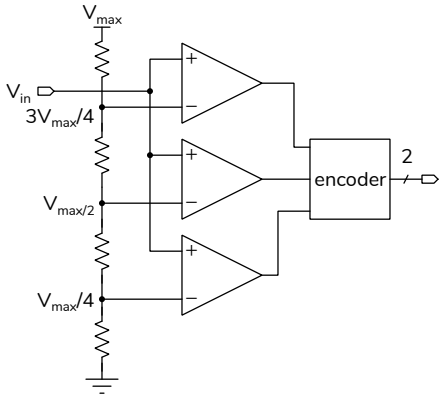
$$\text{period} = T = \frac{1}{10\,kHz} = 100\mu s.$$

$$T_{clock} = \frac{T}{2^n} = \frac{100\mu s}{2^{14}} = \frac{100 \times 10^{-6}}{16384} \approx \frac{100 \times 10^{-6}}{20 \times 10^3} = 5 \times 10^{-9}$$

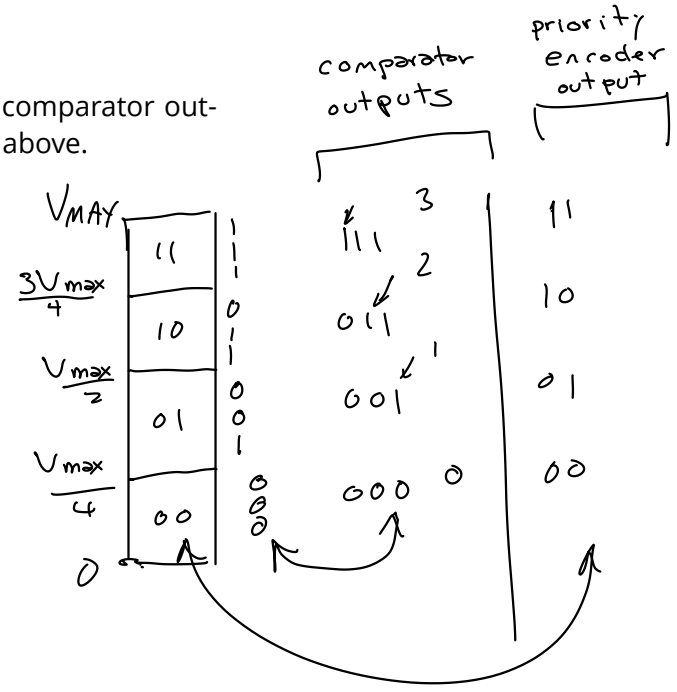
Exercise 9: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

type	speed	complexity or cost: analog	digital
binary weighted	fastest ($f_s = f_{clock}$)	high	low
PWM	$f_s = \frac{f_{clock}}{2^n}$ slower	low	medium
Σ-Δ	($\approx$ same as PWM)	lower	higher

Exercise 10:

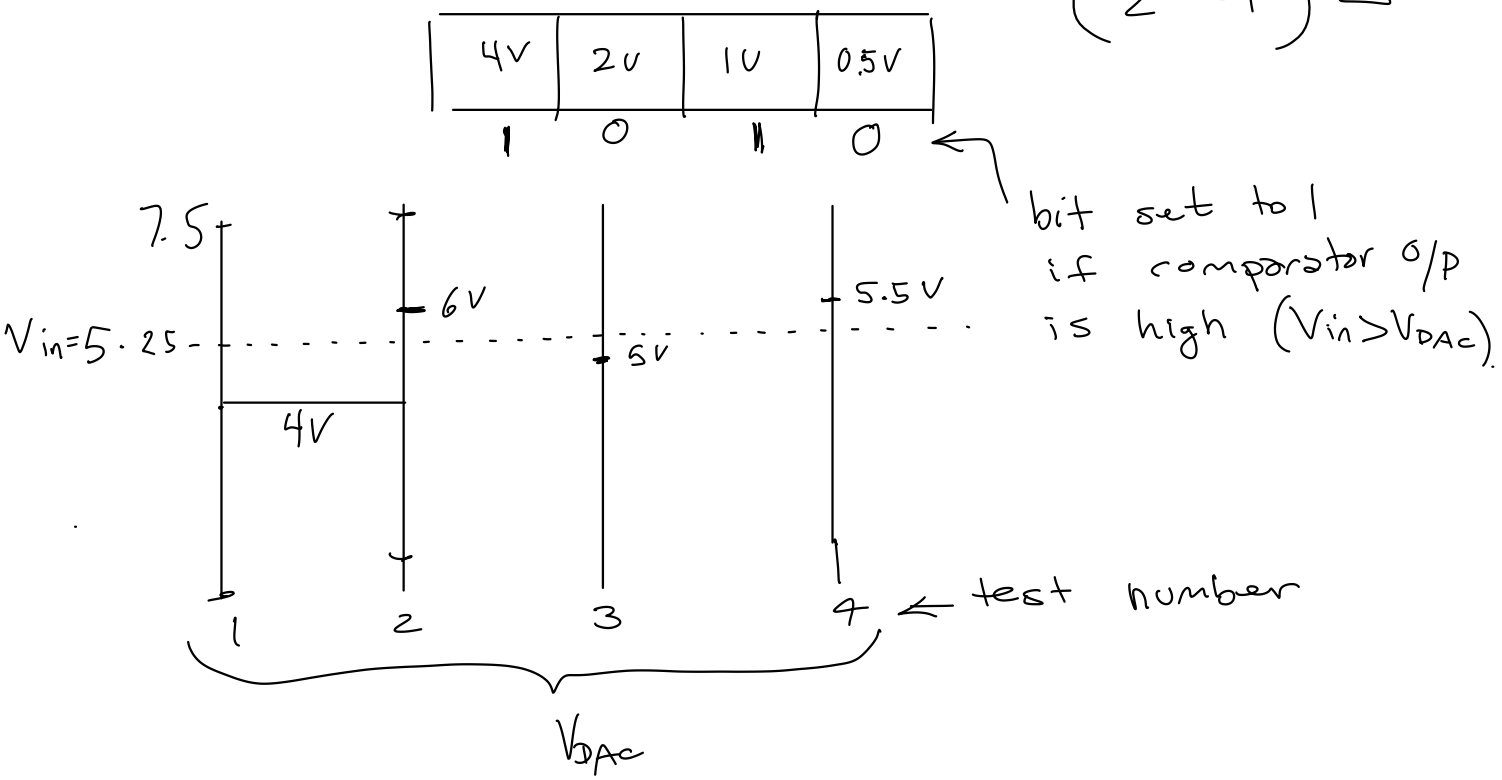


Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

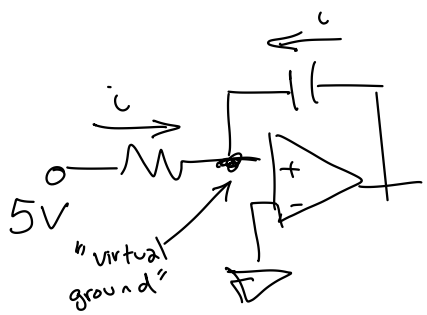


Exercise 11: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output?

range = 0 to $(2^n - 1)\Delta$



Exercise 12: What is the slope of an integrator, in $\mathrm{V/s}$, when charging a 100 nF capacitor with 5 V through a $100\,\mathrm{k\Omega}$ resistor?



$$i = \frac{V}{R} = \frac{5}{100k} = 50\,\mu A$$

$$Q = CV \qquad i = \frac{dq}{dt} = C\frac{dV}{dt}$$

$$\frac{dV}{dt} = \frac{i}{C} = \frac{50 \times 10^{-6}}{0.1 \times 10^{-6}} = 0.5\,mV/\mu s = 500\,V/s.$$

Exercise 13: Rank the different ADCs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

	f_{clock}/f_s	complexity: analog	complexity: digital
flash	1 (fast)	high (2^n comparators)	medium
SAR	n (medium)	medium (accurate R-2R network)	medium
Σ-Δ	2^n (slow)	low	low
dual-slope	2^n (slowest)	low	