

Implementation of Digital Logic Circuits

Exercise 1: Which transistors are on when the output is high? When it is low? In which direction does the output current flow in each case?

Exercise 2: Which of these specifications does the manufacturer guarantee? Which are requirements?

Exercise 3: A logic family has $V_{OH}(\min) = 5 \text{ V}$, $V_{OL}(\max) = 0.5 \text{ V}$, $V_{IH}(\min) = 4 \text{ V}$ and $V_{IL}(\max) = 1.5 \text{ V}$. What are the noise margins?

Exercise 4: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

Exercise 5: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a $10\text{k}\Omega$ resistor pulling up a circuit with 50 pF capacitance to 3.3 V ?

Exercise 6: How many square mm of PCB area does each package require? Which packages have their pins accessible when the packages is placed on the PCB?