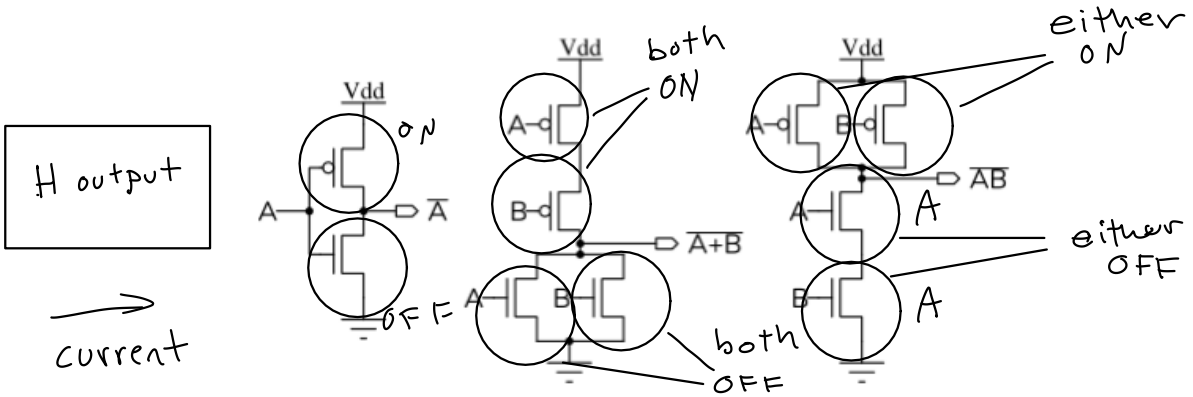
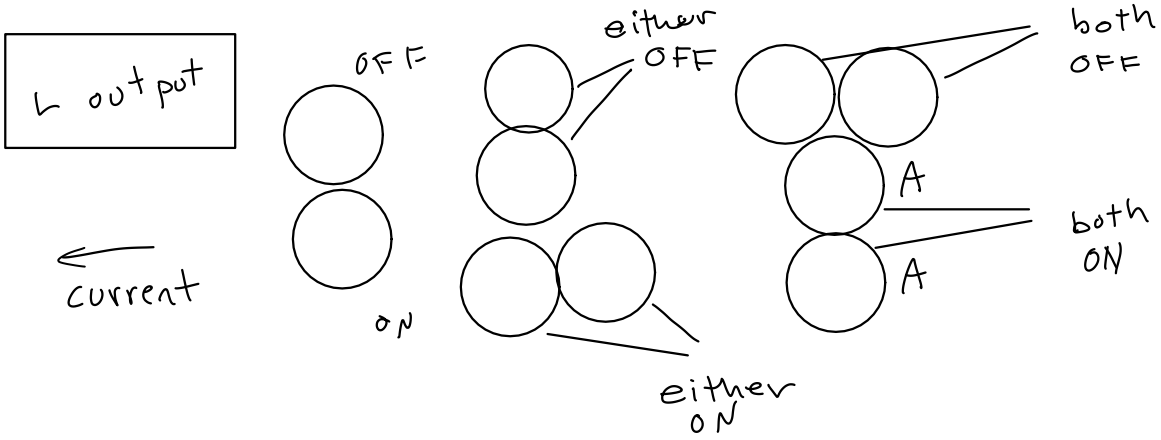
Implementation of Digital Logic Circuits

Exercise 1: Which transistors are on when the output is high? When it is low? In which direction does the output current flow in each case?





Exercise 2: Which of these specifications does the manufacturer guarantee? Which are requirements?

V_{OL}

V_{OH}

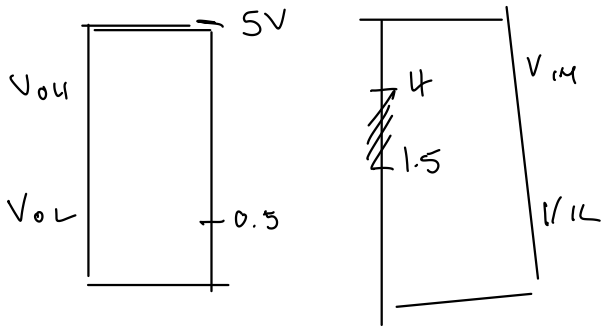
guaranteed

V_{IH}

V_{IL}

requirements (for proper operation)

Exercise 3: A logic family has V_{OH}(min) = 5 V, V_{OL}(max) = 0.5 V, V_{IH}(min) = 4 V and V_{IL}(max) = 1.5 V. What are the noise margins?



← noise margin = 1V
= 5 - 4

← noise margin = 1V
= 1.5 - 0.5

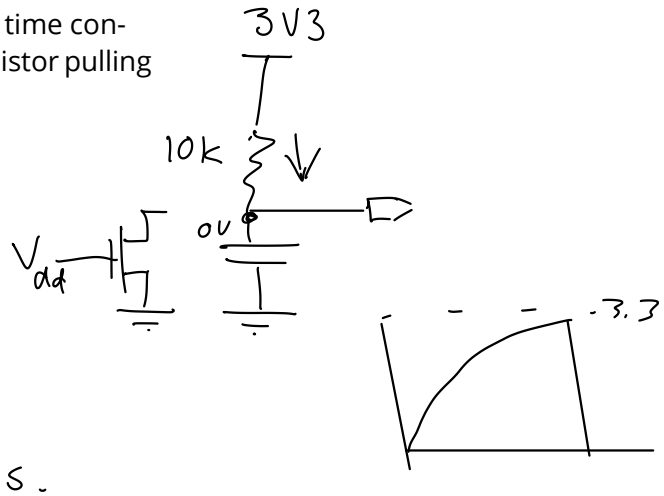
Exercise 4: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

$$\frac{P_2}{P_1} = \frac{f_2}{f_1}\left(\frac{V_2}{V_1}\right)^2 \qquad f_2 = f_1 \qquad V_2 = 3.3 \quad V_1 = 5$$

$$\frac{P_2}{P_1} = 1 \cdot \left(\frac{3.3}{5}\right)^2 = 0.44$$

$$\frac{P_2}{P_1} = \frac{1}{50}\left(\frac{V}{V}\right)^2 = 2\%$$

Exercise 5: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?



$$I = \frac{V}{R} = \frac{3.3}{10k} = 0.33\,mA$$

$$\tau = RC = 10k\Omega \cdot 50pF$$
$$= 10\times10^{3} \cdot 50\times10^{-12}$$
$$= 500\times10^{-9}\,s = 0.5\mu s.$$

Exercise 6: How many square mm of PCB area does each package require? Which packages have their pins accessible when the packages is placed on the PCB?

$22^2 = 484\ mm^2$

$3.5^2 = 12.25 mm^2$

TFQP has accessible pins, BGA does not