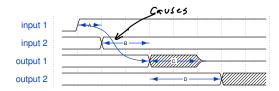
Timing Analysis

Exercise 1:



er?	from	to	
A: C D:	in 2 out 1	in 2 out 1 out 1 out 2	requirenet guaranteed guaranteed guaranteed

Exercise 2: Is t_{PD} a requirement or a guaranteed response?

Exercise 3: Is t_{SU} a requirement or a guaranteed response? How about t_H ?

LSU & the averboth we solved to an input \Rightarrow both we quirements.

Exercise 4:

$$t_{\text{SU}}$$
 (avail) = T_{Clock} - t_{CO} (max) - t_{PD} (max)

Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

Exercise 5: For a particular circuit f_{clock} is 50 MHz, t_{co} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

following a which it will?

$$f_{clock} = 50 \text{ MHz} \rightarrow T_{olock} = \frac{1}{f_{clock}} = \frac{1}{50 \times 106} = 20 \text{ ns.}$$

$$f_{sv} (avail) = T_{olock} - t_{co} - t_{PD}$$

$$= 20 - 2 - 15 = 3 \text{ ns.}$$

$$= 3 + 5 = -2 \text{ ns}$$

$$= 3 + 5 = -2 \text{ ns}$$

$$= 50 \text{ lw for } T_{clock} = 5 \text{ ns} = T_{clock} - t_{co} - t_{PD}$$

$$= 5 + 2 + 15 = 22 \text{ ns}$$

$$f_{clock} = 5 + 2 + 15 = 22 \text{ ns}$$

Exercise 6: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps had times and adder logic that has a 250 ps propagation delay?

Tolock = ?

$$t_{50} = 200 ps$$

 $t_{c0} = 50 ps$
 $t_{pp} = 230 ps$
 $T_{clock} = t_{50} + t_{co} + t_{pp} = 500 ps$
 $2 GHz$