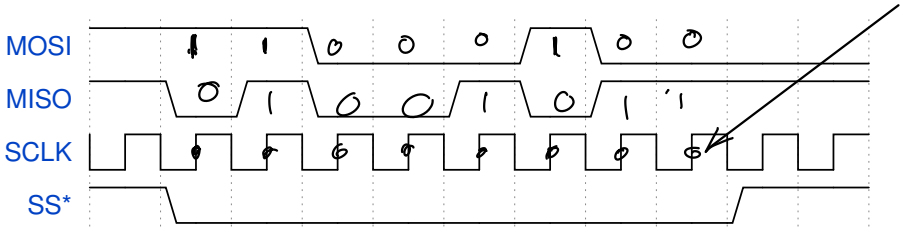
Interfaces

Exercise 1:



MOSI/MISO sampled at rising edge of SCLK

time increases left to right

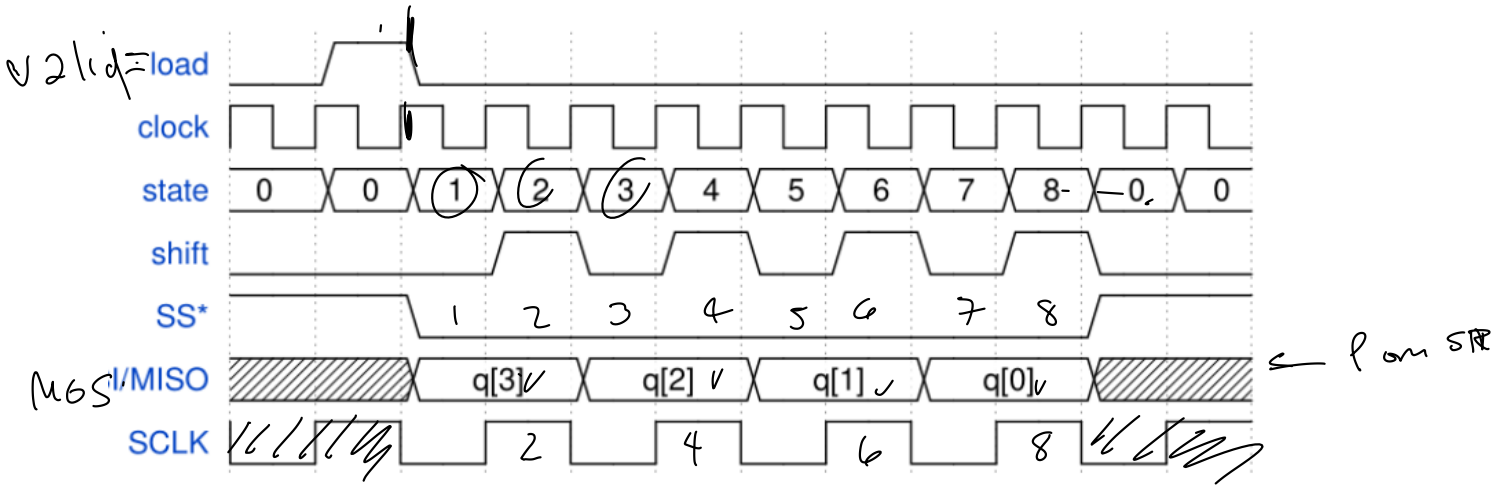
0 1 2 3

The diagram above shows a transfer over an SPI bus. How many bits of data are transferred? What is the value, in decimal, of the data transferred from the master to the slave? From the slave to the master?

8 bits transferred (8 rising edges while $\overline{SS}$ asserted)

MOSI 1100 0100 → 196_{10}

MISO 0100 1011 → 75_{10}



← from STR

Exercise 2

Based on the diagram above, write a state transition table for an SPI interface controller that transfers four bits at a time. Include an idle state. In which states are **SCLK** and **SS** asserted?

state	inputs		next state
	reset	valid	
X	1	X	0 (idle)
0	0	1	1
8	X	X	0
n(≠0)	0	X	n+1

asserted

SCLK: in states 2, 4, 6 & 8

asserted

$\overline{SS}$: in states 1–8