

## **Introduction to Digital Design with Verilog HDL**

**Exercise 1:** What changes would result in a 3-input OR gate?

**Exercise 2:** What schematic would you expect if the statement was  
assign  $y = (a \wedge b) \mid c$  ;?

**Exercise 3:** What are the lengths and values, in decimal, of the following: 4'b1001, 5'd3, 6'h0\_a, 3?

**Exercise 4:** If the signal `i` is declared as `logic [2:0] i;`, what is the 'width' of `i`? If `i` has the value 6 (decimal), what is the value of `i[2]`? Of `i[0]`?

**Exercise 5:** An array declared as `logic [15:0] n;` and has the value `16'h1234`.

What are the values and lengths of the following expressions?

`n[15:13]`

`!n`

`~n[3:0]`

`n>>4`

`n + 1'b1`

`n[7:0] - n[3:0]`

`n >= 16'h1234`

`n ^ ~n`

`n && !n`

`n * ( !n + 1'b1 )`

**Exercise 6:** What is the value of the expression  $3 \cdot 10 \div 20$ ? Of the expression  $x \cdot 1 \div 0$  if  $x$  has the value 0? If  $x$  has the value -1?

**Exercise 7:** Draw the schematics corresponding to:

$y = a ? s1 : b ? s2 : c ? s3 : s4;$

$y = a ? ( b ? s1 : s2 ) : ( c ? s3 : s4 );$

**Exercise 8:** Use slicing and concatenation to compute the byte-swapped value of an array `n` declared as `logic [15:0] n`.



**Exercise 9:** If `n` has the value `16'h1234`, what is the value and length of `{n[7:0], n[15:8], 4'b1111}`?

**Exercise 10:** Use concatenation to shift  $n$  left by two bits.

**Exercise 11:** Use concatenation to assign the high-order byte of  $n$  to  $a$  and the low-order byte to  $b$ .

**Exercise 12:** How would you specify the bit marked A in the diagram above? The bits marked B? The least-significant byte?

**Exercise 13:** Define a Verilog lookup table named `isprime` that can be used to determine if a value between 0 and 7 is a prime number or not. The result should be 1 if the value is a prime or else 0. *Hint: The primes are 2, 3, 5 and 7.*

**Exercise 14:** Write an `always_ff` statement that toggles (inverts) its output on each rising edge of the clock.

**Exercise 15:** Label the signal  $t$  in the schematic.

**Exercise 16:** Rewrite the `ex60` module using operators. Which version – “structural” or “behavioural” – is easier to understand?