D/A and A/D Conversion

Introduction

In this lab you will build a pulse-width modulation (PWM) digital-to-analog converter (DAC) and use it to implement a ramp-type analog-to-digital converter (ADC). The ADC value will be displayed on an LED display. You will test your design by comparing the results to DMM measurements.

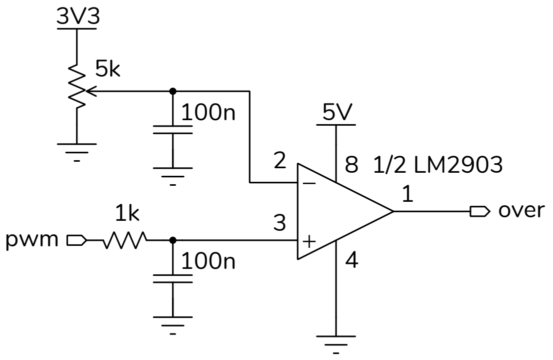
The design is composed of the following modules:

- an 8-bit PWM DAC
- a sawtooth waveform generator
- a multiplexed LED display (provided)

You must design the logic for the DAC and ADC components, integrate it with the supplied code, and demonstrate your design. Block diagrams and descriptions of the DAC and ADC operation are given below.

Circuit

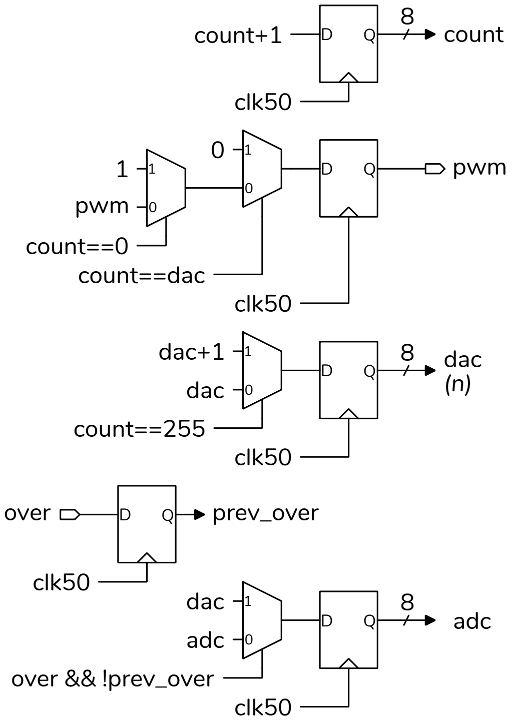
The circuit consists of an RC low-pass filter ($R = 1\,\text{k}\Omega$, $C = 10\,\text{nF}$, $RC = 100\,\mu\text{s}$), an LM2903 dual analog comparator, and a $5\,\text{k}\Omega$ variable resistor that you can adjust to set the analog input voltage to the ADC:



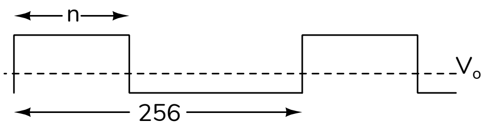
The output is open-collector so a pull-up resistor must be configured on the corresponding CPLD input (**over**).

HDL

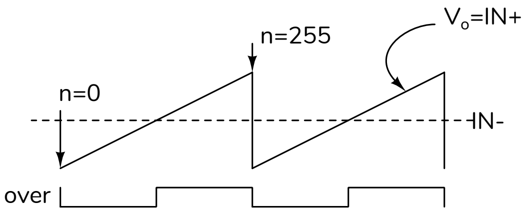
The block diagram below shows an 8-bit PWM DAC and ramp ADC:



An 8-bit counter, **count**, counts continuously from 0 to 255. The one-bit output, **pwm**, is turned on when the counter is zero and is turned off when the counter reaches the current DAC value, n. This results in a waveform whose duty cycle is $D = n/256$ and whose average voltage is $V_o = D \times 3.3\,\text{V}$ (for a high-level digital output voltage of 3.3 V). The RC filter smooths out the pulses, resulting in a DC voltage of V_o (with a bit of "ripple").



The value of n is defined by another 8-bit counter (labelled **dac** above). This counter is incremented by 1 each time the PWM counter reaches 255. This results in the value of n increasing from 0 to 255 and then “wrapping around” back to zero. This produces a “sawtooth” waveform consisting of “ramps”.

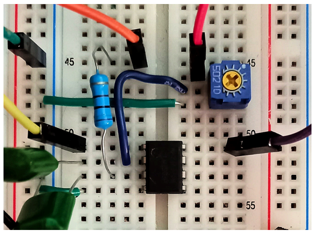


The output of the comparator, labelled **over**, is high when the voltage at IN+ is higher than the voltage at IN− and low otherwise.

When the DAC output ramp reaches the analog input voltage being measured, the comparator output, **over**, goes from low to high. On the rising edge of **over** the value of **dac** is captured. This is passed on to the LED display module (supplied and not shown here).

Procedure

Build the circuit shown in the schematic above. For example:



In the sample files, **pwm** is output on the CPLD's pin 1 and **over** is input on pin 3. The +5, +3.3 supplies and ground are available on the connectors on the top right of the board.

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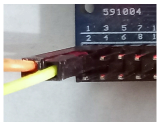
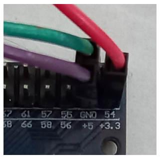




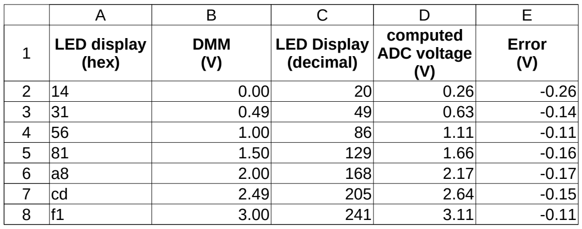
Fill in the **lab8.sv** file with the code required to implement the DAC and ADC described above, compile your design, and program the CPLD.

Connect the CPLD and power it on. Adjust the variable resistor as you measure the DC voltage with a DMM at the IN− comparator input. You should be able to adjust the voltage from 0 to 3.3 V.

Measure the AC and DC voltages at the IN+ comparator input. For an ideal sawtooth the DC value should be approximately 1.65 V and the RMS AC voltage be about 950 mV. The screen capture in Figure 1 shows an example of the waveform measured at the IN+ comparator input and an example of the DC and AC voltages measured:

The LED display should show two hex digits corresponding to the analog input voltage (ideally, 00 for 0 V through FF for 3.3 V).

Prepare a table as shown below recording the hex value on the LED display, the comparator IN+ voltage from the variable resistor as measured with a DMM, the predicted voltage corresponding to the hex value assuming ideal DAC and ADC operation[1], and the difference between the predicted and measured values.

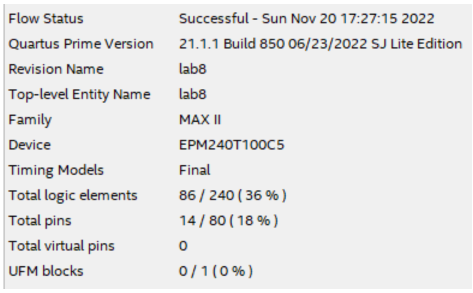


	A	B	C	D	E
1	LED display (hex)	DMM (V)	LED Display (decimal)	computed ADC voltage (V)	Error (V)
2	14	0.00	20	0.26	-0.26
3	31	0.49	49	0.63	-0.14
4	56	1.00	86	1.11	-0.11
5	81	1.50	129	1.66	-0.16
6	a8	2.00	168	2.17	-0.17
7	cd	2.49	205	2.64	-0.15
8	f1	3.00	241	3.11	-0.11

Report

Submit a report to the appropriate assignment folder, in PDF format, that includes the following:

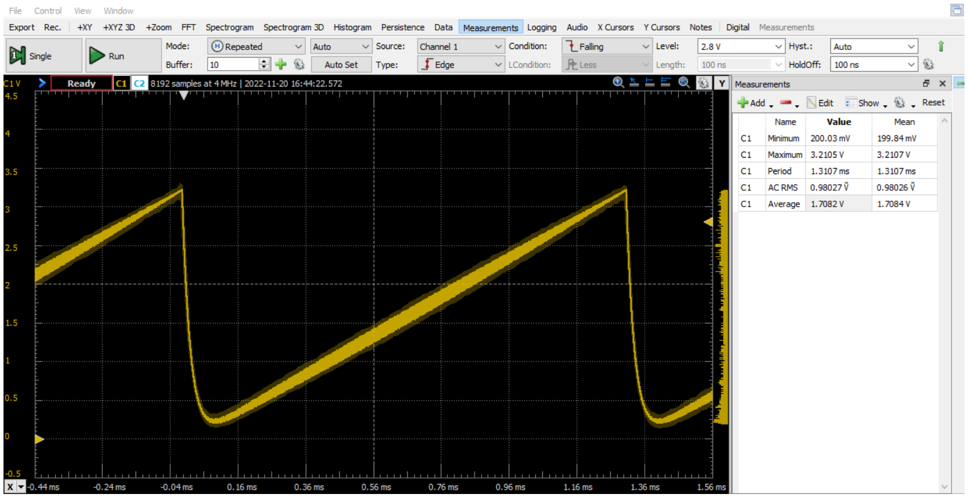
- A listing of your Verilog code. Follow the course coding guidelines.
- A compilation report similar to:



Flow Status	Successful - Sun Nov 20 17:27:15 2022
Quartus Prime Version	21.1.1 Build 850 06/23/2022 SJ Lite Edition
Revision Name	lab8
Top-level Entity Name	lab8
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	86 / 240 (36 %)
Total pins	14 / 80 (18 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

- The schematic generated from Tools > RTL Netlist such as that in Figure 2.

[1] If your are using a spreadsheet the HEX2DEC function may be useful.



Mode: Repeated | Auto
Buffer: 10
Source: Channel 1
Type: Edge
Condition: Falling
LCondition: Less
Level: 2.8 V
Length: 100 ns
Hyst.: Auto
HoldOff: 100 ns

Ready | C1 | C2 | 8192 samples at 4 MHz | 2022-11-20 16:44:22.572

Measurements

	Name	Value	Mean
C1	Minimum	200.03 mV	199.84 mV
C1	Maximum	3.2105 V	3.2107 V
C1	Period	1.3107 ms	1.3107 ms
C1	AC RMS	0.98027 Ṽ	0.98026 Ṽ
C1	Average	1.7082 V	1.7084 V

Figure 1: Screen capture showing the sawtooth waveform at the DAC output and various voltage measurements

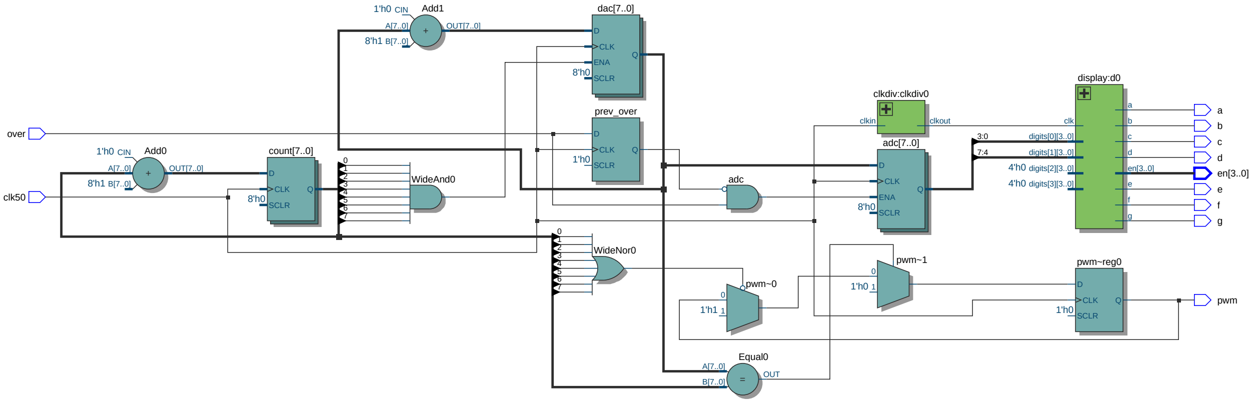


Figure 2: Synthesis results generated by Quartus.

- A table similar to that above showing your ADC results and the corresponding DMM voltages.

- A brief explanation of why the ADC outputs do not match the voltages measured with the DMM (*Hint: What is the range of voltages for the sawtooth waveform in the 'scope screen capture above? What are V_{OL} and V_{OH} for Intel MAX II CPLDs?*[2])

If you do not demo your circuit in the lab, submit a video to the appropriate assignment folder showing both the LED and DMM results simultaneously as you adjust the input voltage from 0 to 3.3 V. An example video is available on the course website.

Hints

Measuring the comparator inputs and outputs with a 'scope or DMM may help you narrow down any problems.

Results may be incorrect for inputs above 3 V because the comparator operation is only specified for inputs up to supply voltage minus 2 V ($5 - 2 = 3$ V).

[2] See Table 5-5 of the MAX II datasheet available on the course website.