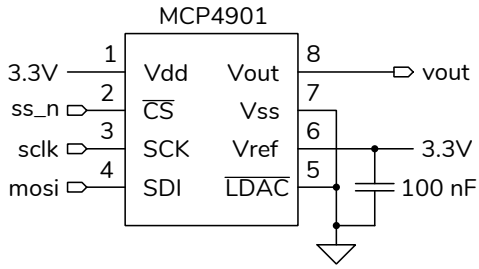
SPI Interface

Revision 2: added bypass capacitor, MISO delay to block diagram, simulation example, and use of keypad 2 to reset.

Introduction

In this lab you will design and implement an SPI interface. You will use it to set the output voltage of an MCP4901 8-bit digital-to-analog converter (DAC).

The MCP4901 has the following pinout:



- V_{dd} and V_{ss} are the digital supply (3.3 V) and ground voltages respectively
- V_{ref} is the maximum analog output level. This will be connected to the 3.3 V supply.
- V_{out} is the analog voltage output whose value is $V_{ref} \times {}^{d}/_{256}$ where d is the 8-bit digital value written to the DAC.
- $\overline{CS}$, SCK and SDI, correspond to the $\overline{SS}$, SCLK and MOSI SPI interface signals
- $\overline{LDAC}$ should be set low

The value written to the MPC4901 must be a 16-bit value constructed as defined as in the diagram below taken from its Datasheet:

REGISTER 5-3: WRITE COMMAND REGISTER FOR MCP4901 (8-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
0	BUF	$\overline{GA}$	$\overline{SHDN}$	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x
bit 15															bit 0

The most significant 4 bits should be set to 0011.

In this lab you will connect the DAC's SPI interface to your CPLD, implement an SPI interface on the CPLD and use it to set the DAC's output voltage to a value determined by the digits of your BCIT ID. You will measure the analog voltage output with a DMM to verify the correct operation of the interface.

You will be supplied with a module that instantiates your SPI interface which should operate as shown below (from the lecture notes on Interfaces):

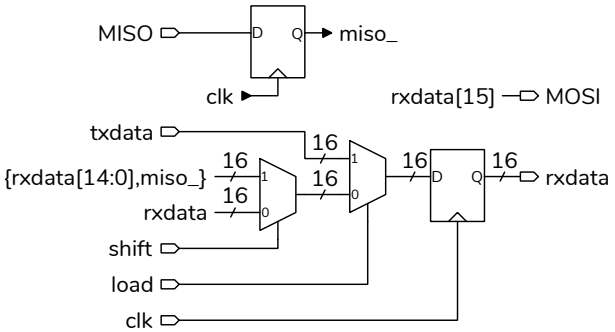


Figure 1 below shows the signals generated by the SPI transmitter (**mosi**, **ss_n** and **sclk**). Figure 2 shows simulation results when writing the value 16'h3B20 as in the example below and reading the value 16'hAAAA.

Requirements

Pushing keypad key [1] should result in an analog value being output that is equal to the last two digits of your student ID modulo 33 (the remainder after dividing by 33) divided by 10. For example if your student ID were A00123456 then 56 modulo 33 = 23 and the output voltage should be 2.3 V.

The analog output voltage is given by the equation:

$$V_{out} = V_{ref} \frac{d}{256}$$

where d is the 8-bit integer written to the DAC in bits 11 through 4 of the 16-bit word. For example, to obtain a 2.3 V output the value d would be:

$$d = 256 \frac{V_{out}}{V_{ref}} = 256 \frac{2.3}{3.3} = 178 = 8'b1011\_0010$$

and the 16-bit word written to the DAC would be 16'b0011_1011_0010_0000.

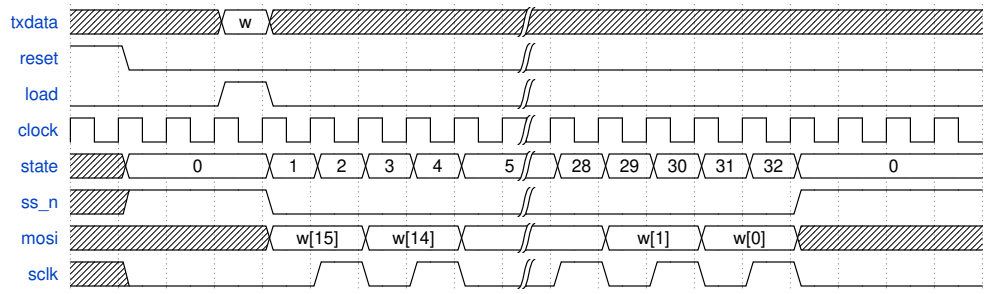


Figure 1: SPI Interface Signals (16 bits).

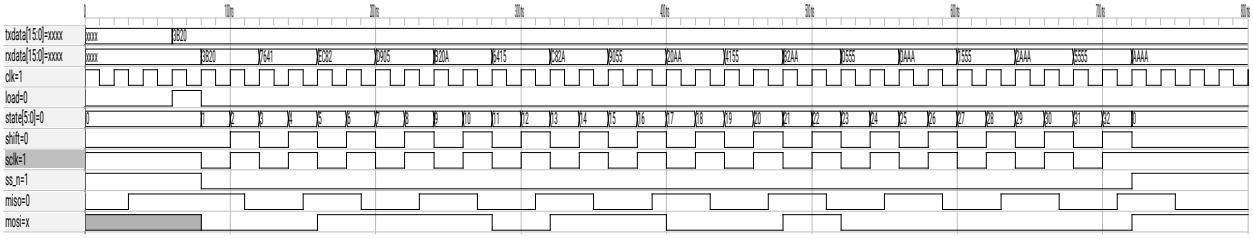
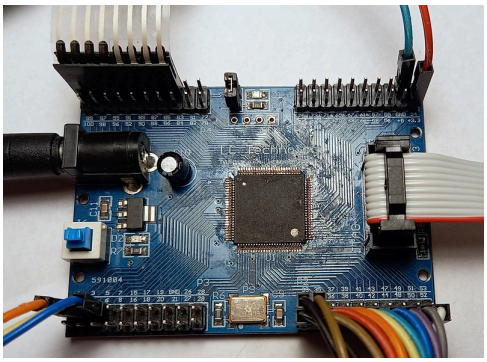
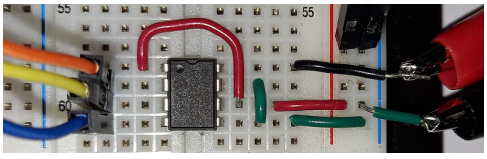


Figure 2: Simulation Results.

CPLD I/O

The following photos shows the connections between the CPLD board and prototyping board.





The **row**, **col** and **clk50** pin connections are the same as in previous labs. The following additional pin assignments are suggested:

CPLD Pin	MPC4901 Pin	Signal Name
1	2	**ss_n**
3	3	**sclk**
5	4	**mosi**

A **lab6.qsf** file is available on the course web site with these pin assignments.

The ground and 3.3 V connections can be made to the pins at the top right of the CPLD board. The 100 nF bypass capacitor will reduce noise on V_{dd} and V_{ref}. Do *not* use external power supplies.

Procedure

Create a Quartus project named **lab6** and add the file **lab6.sv**.

Add code to the Verilog module named **spi** to implement the block diagram shown above. Edit the line **txdata <= 16'b....** and insert the value corresponding to your BCIT ID.

Wire up the MCP4901 DAC from your ELEX 2117 parts kit as shown above and connect power, ground, and the sclk, mosi and $\overline{ss}$ signals to the appropriate CPLD board pins.

Connect a DMM to V_{out} to measure the output voltage. Pressing the [1] key should result in the DMM displaying the appropriate voltage for your stu-

dent number. Pressing the 2 key should result in the DMM displaying 0 V.

The supplied **`lab6.sv`** file also contains a test-bench (**`lab6_tb`**) that you can use to troubleshoot your design with the test vector file (**`lab6tv.csv`**) on the course web site.

Submission

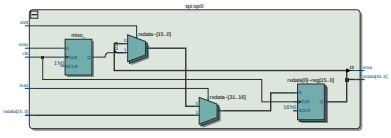
To get credit for completing this lab, submit the following to the appropriate Assignment folder on the course website:

- A PDF document containing:

    1. The calculation of the required output voltage corresponding to your BCIT ID and the 16-bit value that you need to write to the DAC, computed as described above.
    2. A listing of your Verilog code for the **`spi`** module (include only the **`spi`** module, not the other code supplied).
    3. A screen capture of your compilation report (Window > Compilation Report) similar to:

Flow Status	Successful - Tue Nov 8 21:03:45 2022
Quartus Prime Version	21.1.1 Build 850 06/23/2022 SJ Lite Edition
Revision Name	lab6
Top-level Entity Name	lab6
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	48 / 240 (20 %)
Total pins	14 / 80 (18 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

    4. A screen capture of the schematic created by Tools > Netlist Viewers > RTL Viewer, showing only the **`spi`** module (use the + button). For example:



- If you do not demonstrate your completed lab in person, submit a short video showing the DMM voltage reading when you press the 2 and 1 keys.