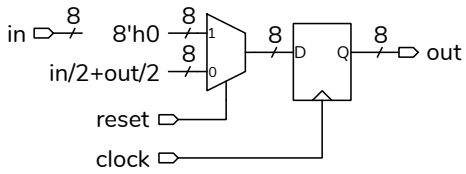
Simulation

Introduction

In this lab you will simulate the operation of a circuit whose output on each clock edge is half of the current input plus half of the previous output:



This is an example of an Infinite Impulse Response (IIR) filter.

Your test vectors will have a reset input, an 8-bit **`in`** input and the expected 8-bit **`out`** output. The first test vector should assert **`reset`**. Then **`in`** should be the value 255 repeated four times, the value zero repeated six times, and the eight digits of you student ID multiplied by 10.

The expected outputs can be computed using a spreadsheet and exported as a **`.csv`** file. For an ID of A00123456 the test vector file would be:

```
1,0,0
0,255,127
0,255,190
0,255,222
0,255,238
0,0,119
0,0,59
0,0,29
0,0,14
0,0,7
0,0,3
0,0,1
0,0,0
0,10,5
0,20,12
0,30,21
0,40,30
0,50,40
0,60,50
```

Procedure

Create a spreadsheet that computes the test vector values for your student ID and export the values as a **`.csv`** file. The course website has a sample spreadsheet. Note that integer division in Verilog truncates so the spreadsheet formula must do the same.

Write a module that implements the IIR filter described above. Remember to follow the course coding guidelines, including adding a comment at the beginning of the file with your name and the date.

Write a testbench that instantiates your IIR filter, and simulates your design using your test vectors. You can follow the example in the lecture notes.

Follow the procedure in Software Installation and Use document and the video on the course web site to create a simulation project, add the file(s) with your modules to the project and compile them. Add the **`reset`**, **`in`**, **`clock`**, and **`out`** signals to the Wave window. Run the simulation. The Transcript window should show any messages generated by the testbench and the Wave window should show the signal waveforms.

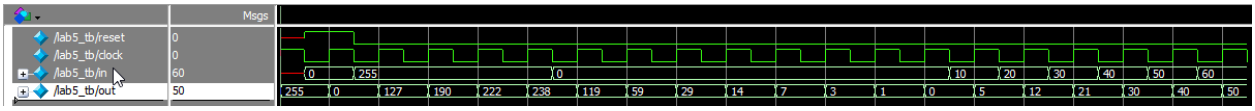


Figure 1: Example simulation waveforms.

Report

Submit a PDF file to the appropriate Assignment folder that includes the following:

- a listing of your test vector file
- listings of your testbench and DUT modules
- a screen capture of the waveforms similar to that in Figure 1 (right-click on the waveform and select Radix as Unsigned for **`in`** and **`out`**).
- a screen capture of the Transcript window showing the messages generated by running the simulation. For example:

```
VSIM 5> run -all
# Error: 0  60  50 51
# ** Note: $finish    : C:/Users/Ed/2117/lab5/lab5_tb.sv(41)
#    Time: 19500 ns  Iteration: 2  Instance: /lab5_tb
# 1
# Break in Module lab5_tb at C:/Users/Ed/2117/lab5/lab5_tb.sv line 41
```