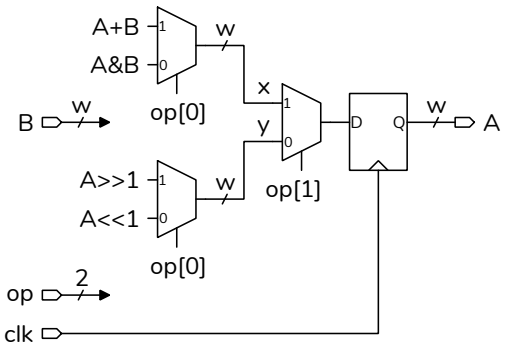
Solutions to Final Exam

Question 1

Write a Verilog module named **alu** corresponding to the diagram shown below. The module has a **w**-bit input **B**, a 2-bit input **op**, a clock input **clk**, and a **w**-bit registered output **A**. The module declaration should include a parameter named **w** for the bus widths with a default value of 16. The use of the signals **x** and **y** is optional but they must be declared if they're used. Bits should be numbered in decreasing order. Follow the course coding conventions. You may omit comments.



Answer

An answer using **x** and **y** is:

```
module alu
  #(parameter w=16)
  ( input logic [w-1:0] B,
    input logic [1:0] op,
    input logic clk,
    output logic [w-1:0] A ) ;

   logic [w-1:0] x, y ;

   assign x = op[0] ? A+B : A&B ;
   assign y = op[0] ? A>>1 : A<<1 ;

   always @(posedge clk) A
     <= op[1] ? x : y ;

endmodule
```

Question 2

Fill in the table below with the value of the each expression. Give the answers as Verilog numeric literals including the length and using a hexadecimal base. Assume the following declarations:

```
logic [7:0] x = 8'ha5 ;
```
(or `logic [7:0] x = 8'h5a ;`)
```
logic [3:0] y = 4'b0011 ;
```

expression	value
`{x[3:0],x[7:4]}`	
`!x||x`	
`~x|x`	
`x >> 1 + 1'b1`	
`2*y`	
`x[1:0] > y`	
`x^y`	
`!y ? x : x^y`	

Answer

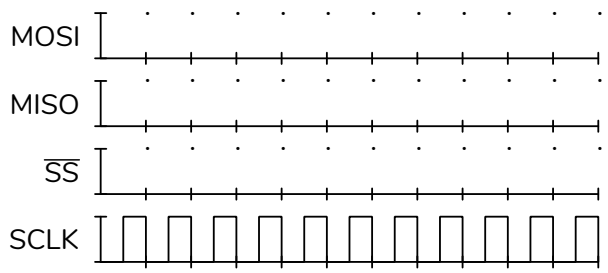
The following values were calculated by Modelsim:

```
    logic [3:0] y = 4'b0011 ;

for logic [7:0] x = 8'ha5 ;

{x[3:0],x[7:4]}: value: 8b'01011010 = 8'h5a
        !x || x: value: 1b'1 = 1'h1
         ~x | x: value: 8b'11111111 = 8'hff
  x >> 1 + 1'b1: value: 8b'00101001 = 8'h29
           2*y: value: 32b'0110 = 32'h00000006
     x[1:0] > y: value: 1b'0 = 1'h0
           x^y: value: 8b'10100110 = 8'ha6
   !y ? x : x^y: value: 8b'10100110 = 8'ha6

for logic [7:0] x = 8'h5a ;

{x[3:0],x[7:4]}: value: 8b'10100101 = 8'ha5
        !x || x: value: 1b'1 = 1'h1
         ~x | x: value: 8b'11111111 = 8'hff
  x >> 1 + 1'b1: value: 8b'00010110 = 8'h16
           2*y: value: 32b'0110 = 32'h00000006
     x[1:0] > y: value: 1b'0 = 1'h0
           x^y: value: 8b'01011001 = 8'h59
   !y ? x : x^y: value: 8b'01011001 = 8'h59
```

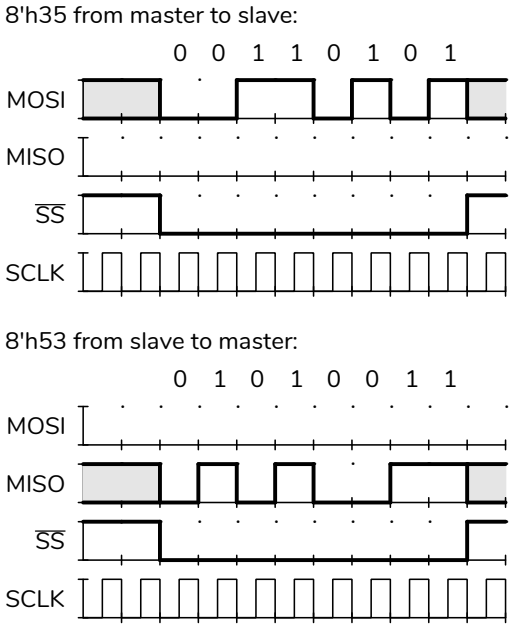
The most common error was not noticing that addition has higher precedence than right shift in the fourth expression. Another common error was not noticing that the literal 2 has a length of 32 bits and thus so does the result (in the fifth expression).

Question 3

Draw the waveforms that would be used to transfer a byte that has the value `8'h35` (or `8'h53`) (in Verilog notation) from the master to the slave (or slave to the master) over an SPI interface. Draw the waveforms for $\overline{\texttt{SS}}$, and the appropriate data signal (either `MOSI` or `MISO`, but not both). Follow the conventions shown in the lecture notes, including the timing of $\overline{\texttt{SS}}$ relative to the data, the data relative to `SCLK`, and that the most significant bit is transferred first.



Answer



Question 4

A 5 V TTL IC has V_{IH} of 2 V and V_{IL} of 0.5 V. It is driven by a 3.3 V CMOS IC that has V_{OH} of 3.2 V and V_{OL} of 0.3 (or 0.6) V. What are the noise margins? Will this interface work correctly?

Answer

The high noise margin is $V_{OH} - V_{IH} = 3.2 - 2 = \boxed{1.2\text{ V}}$.

For $V_{OL} = 0.3$ V the low noise margin is $V_{IL} - V_{OL} = 0.5 - 0.3 = \boxed{0.2\text{ V}}$ and the interface $\boxed{\text{will}}$ work correctly.

For $V_{OL} = 0.6$ V the low noise margin is $V_{IL} - V_{OL} = 0.5 - 0.6 = \boxed{-0.1\text{ V}}$ (or 0.1). The interface $\boxed{\text{will not}}$ work correctly because V_{OL} must be lower than V_{IL} for low output levels to be recognized as low.

Question 5

A logic circuit operates at a clock rate of 20 (or 10) MHz. The propagation delays through the combinational logic paths from flip-flop outputs to flip-flop inputs range from 10 to 25 ns. The flip-flop clock-to-output delay, t_{CO}, is 20 ns and the required minimum setup time is t_{SU}= 10 ns. What is the slack? Will this circuit work reliably?

Answer

$T_{\text{clock}} = {}^{1}/_{f_{\text{clock}}} = {}^{1}/_{20\,\text{MHz}} = 50$ ns (or 100 ns).

$$\begin{aligned} t_{SU}(\text{avail}) &= T_{\text{clock}} - t_{CO}(\text{max}) - t_{PD}(\text{max}) \\ &= 50 - 20 - 25 = 5 \end{aligned}$$

(or $t_{SU}(avail) = 100 - 20 - 25 = 55$).

$$\begin{aligned} \text{slack} &= t_{SU}(\text{available}) - t_{SU}(\text{required}) \\ &= 5 - 10 = -5 \end{aligned}$$

and it $\boxed{\text{won't}}$ work reliably. For a 10 MHz clock slack $= 55 - 10 = 45$ and it $\boxed{\text{will}}$ work reliably.

Question 6

An engine vibration analyzer needs to sample and digitize an analog sensor signal with a voltage between -1 and 1 volts that contains frequencies up to 100 (or 200) Hz.

(a) What sampling rates would avoid aliasing?

(b) How many *bits* of resolution are required if the voltage resolution – the difference between quantized values – must be less than 10 (or 5) mV? Your answer should be an integer.

Answer

(a) The sampling rate should be more than twice the highest frequency: > 200 (or > 400) Hz.

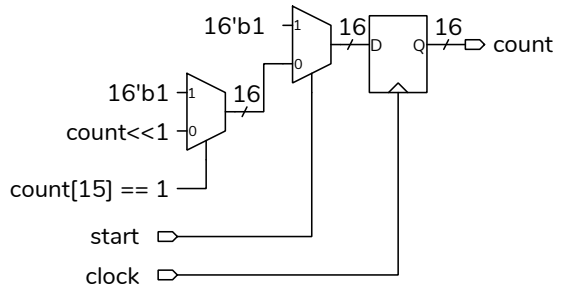
(b) The voltage range is $V = 2\ V$ so the voltage resolution is $\Delta = V/(2^n - 1)$ so $n = \log_2(2/0.01) = \log_2(200) \approx 7.6$ so 8 bits are needed. For a 5 mV voltage resolution 9 bits are needed.

Question 7

Draw a block diagram for the following Verilog module. Follow the course conventions for block diagrams.

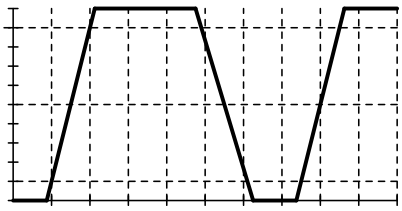
```
module exam
   ( input logic start, clock,
     output logic [15:0] count ) ;

   always_ff @(posedge clock) count
     <= start ? 16'b1 :
        count[15] == 1'b1 ? 16'b1 :
        count << 1 ;

endmodule
```

Answer



Question 8

The following diagram shows an oscilloscope screen capture that includes one period of a digital waveform. The scale on the horizontal axis is 10 (or 20) ns per division. What are the values of the following (give your answers in nanoseconds):



(a) rise time:

(b) negative pulse width:

(c) period:

Answer

(a) Rise time is measured from 10% to 90% of the maximum voltage. In this case it's one division: 10 (or 20) ns.

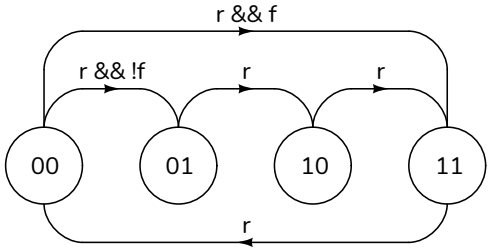
(b) The negative pulse width is measured at 50% of the maximum voltage. In this case it's 2.5 divisions or 25 (or 50) ns.

(c) The period is measured between any two of the same points on the periodic signal. For example, measuring between the 50% crossings, it's 6.5 divisions, 65 (or 130) ns.

Question 9

Write the state transition table for a state machine that has the following state transition diagram. The value in each state circle is the 2-bit binary encoding of that state. The Verilog expression above a state transition defines the condition for a transition between the two states. Conditions that do not result in a change of state are not shown.

Include columns for the current state, the `r` and `f` inputs and the next state. You may use the conventions described in the lecture notes including `x` for "don't-care." You need not include input conditions that do not result in a change of state.



Answer

current state	inputs r	inputs f	next state
00	1	0	01
00	1	1	11
01	1	x	10
10	1	x	11
11	1	x	00