ELEX 2117 : Digital Techniques 2
2022 Fall Term

FINAL EXAM
14:30 – 17:30
Tuesday, December 6, 2022
SW09-110

This exam has nine (9) questions on three (3) pages. The marks for each question are as indicated. There are a total of thirty-eight (38) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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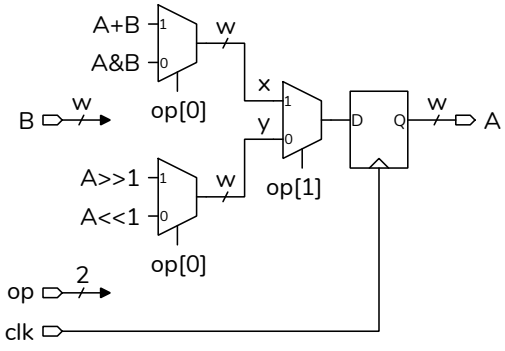
Question 1 — 6 marks

Write a Verilog module named **`alu`** corresponding to the diagram shown below. The module has a **`w`**-bit input **`B`**, a 2-bit input **`op`**, a clock input **`clk`**, and a **`w`**-bit registered output **`A`**. The module declaration should include a parameter named **`w`** for the bus widths with a default value of 16. The use of the signals **`x`** and **`y`** is optional but they must be declared if they're used. Bits should be numbered in decreasing order. Follow the course coding conventions. You may omit comments.



Question 2 — 8 marks

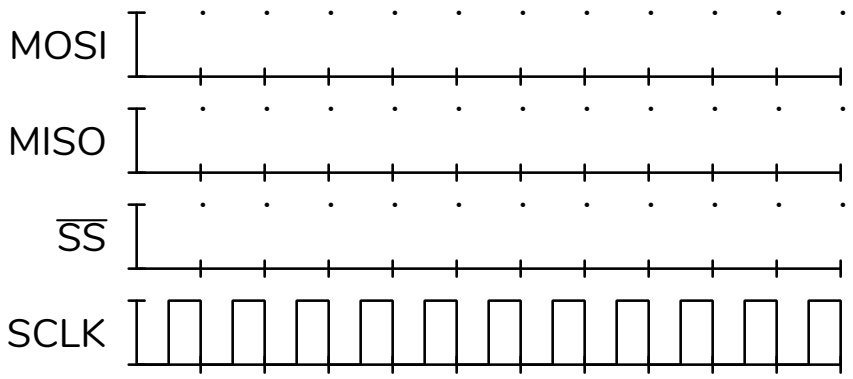
Fill in the table below with the value of the each expression. Give the answers as Verilog numeric literals including the length and using a hexadecimal base. Assume the following declarations:

```
logic [7:0] x = 8'h5a ;
logic [3:0] y = 4'b0011 ;
```

expression	value
`{x[3:0],x[7:4]}`	
`!x||x`	
`~x|x`	
`x >> 1 + 1'b1`	
`2*y`	
`x[1:0] > y`	
`x^y`	
`!y ? x : x^y`	

Question 3 — 5 marks

Draw the waveforms that would be used to transfer a byte that has the value `8'h53` (in Verilog notation) from the slave to the master over an SPI interface. Draw the waveforms for $\overline{\texttt{SS}}$, and the appropriate data signal (either `MOSI` or `MISO`, but not both). Follow the conventions shown in the lecture notes, including the timing of $\overline{\texttt{SS}}$ relative to the data, the data relative to `SCLK`, and that the most significant bit is transferred first.



Question 4 — 2 marks

A 5 V TTL IC has V_{IH} of 2 V and V_{IL} of 0.5 V. It is driven by a 3.3 V CMOS IC that has V_{OH} of 3.2 V and V_{OL} of 0.6 V. What are the noise margins? Will this interface work correctly?

Question 5 — 4 marks

A logic circuit operates at a clock rate of 10 MHz. The propagation delays through the combinational logic paths from flip-flop outputs to flip-flop inputs range from 10 to 25 ns. The flip-flop maximum clock-to-output delay, t_{CO}, is 20 ns and the required minimum setup time is t_{SU}= 10 ns. What is the slack? Will this circuit work reliably?

Question 6 — 2 marks

An engine vibration analyzer needs to sample and digitize an analog sensor signal with a voltage between −1 and 1 volts that contains frequencies up to 200 Hz.

(a) What sampling rates would avoid aliasing?

(b) How many *bits* of resolution are required if the voltage resolution – the difference between quantized values – must be less than 5 mV? Your answer should be an integer.

Question 7 — 3 marks

Draw a block diagram for the following Verilog module. Follow the course conventions for block diagrams.

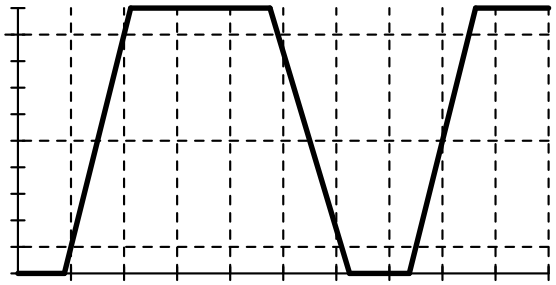
```
module exam
   ( input logic start, clock,
     output logic [15:0] count ) ;

   always_ff @(posedge clock) count
     <= start ? 16'b1 :
        count[15] == 1'b1 ? 16'b1 :
        count << 1 ;

endmodule
```

Question 8 — 3 marks

The following diagram shows an oscilloscope screen capture that includes one period of a digital waveform. The scale on the horizontal axis is 20 ns per division. What are the values of the following (give your answers in nanoseconds):



(a) rise time:

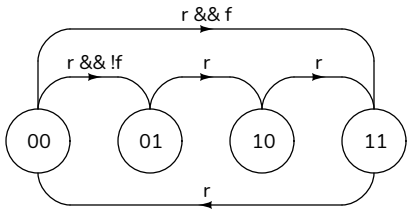
(b) negative pulse width:

(c) period:

Question 9 — 5 marks

Write the state transition table for a state machine that has the following state transition diagram. The state machine has two one-bit inputs: `r` and `f`. The value in each circle is the 2-bit binary encoding of that state. The Verilog expression above a state transition defines the condition for a transition between the two states. Conditions that do not result in a change of state are not shown.

Include columns for the current state, the `r` and `f` inputs, and the next state. You may use the conventions described in the lecture notes including `x` for "don't-care." You need not include input conditions that do not result in a change of state.



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Sample Exam 2 A01234567

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Question 1 — 6 marks

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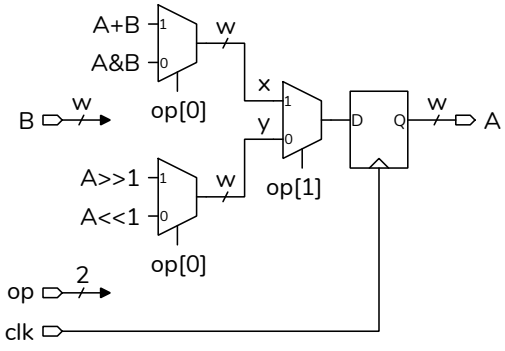

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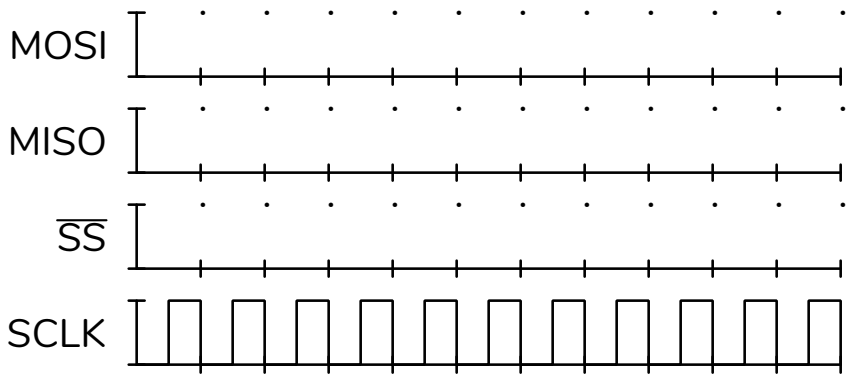
```
logic [7:0] x = 8'ha5 ;
logic [3:0] y = 4'b0011 ;
```

expression	value
`{x[3:0],x[7:4]}`	
`!x||x`	
`~x|x`	
`x >> 1 + 1'b1`	
`2*y`	
`x[1:0] > y`	
`x^y`	
`!y ? x : x^y`	

Question 3 — 5 marks

Draw the waveforms that would be used to transfer a byte that has the value `8'h35` (in Verilog notation) from the master to the slave over an SPI interface. Draw the waveforms for $\overline{\texttt{SS}}$, and the appropriate data signal (either `MOSI` or `MISO`, but not both). Follow the conventions shown in the lecture notes, including the timing of $\overline{\texttt{SS}}$ relative to the data, the data relative to `SCLK`, and that the most significant bit is transferred first.



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An engine vibration analyzer needs to sample and digitize an analog sensor signal with a voltage between −1 and 1 volts that contains frequencies up to 100 Hz.

(a) What sampling rates would avoid aliasing?

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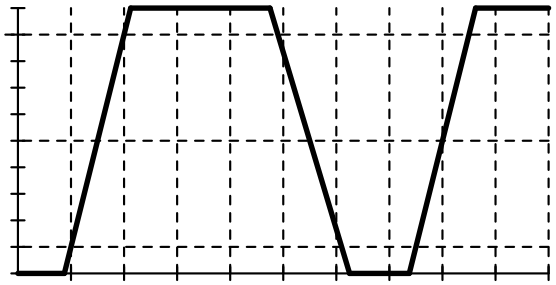

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