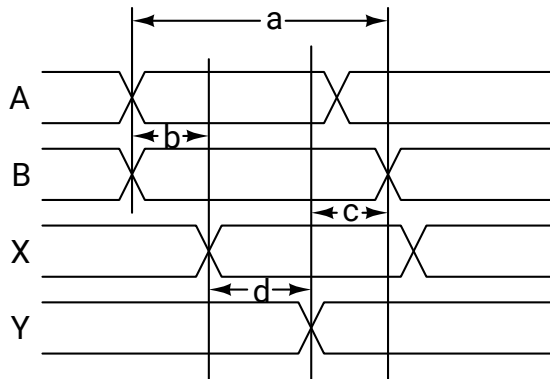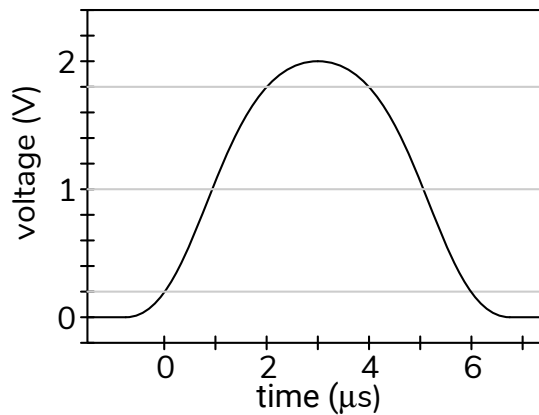1. A datasheet contains the following timing diagram. **A** and **B** are inputs, **X** and **Y** are outputs. List the letters corresponding to the timing requirements that your design must meet.

2. You measure the following waveform using an oscilloscope. What are (a) the (10% to 90%) rise time of the signal, and (b) the positive pulse duration? Your answers must include units.

3. A clock divider uses a counter that counts down from $N - 1$ to zero. The clock frequency used to update the counter is 20 MHz and the divided clock frequency is 400 kHz. What is N?

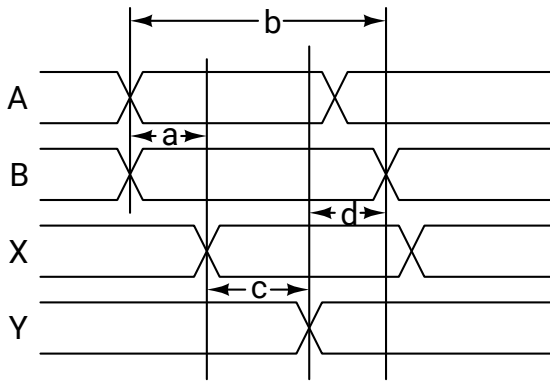4. A module is declared as:　　**`module foo ( logic [15:0] a, b, c ) ;`**

Three of these modules are instantiated as follows:

```
logic [15:0] a=1, b=2, c=3 ;
foo f0 ( .* ) ;
foo f1 ( .a(b), .b, .c(15'd4) ) ;
foo f2 ( .b(c), .a(15'd1), .* ) ;
```
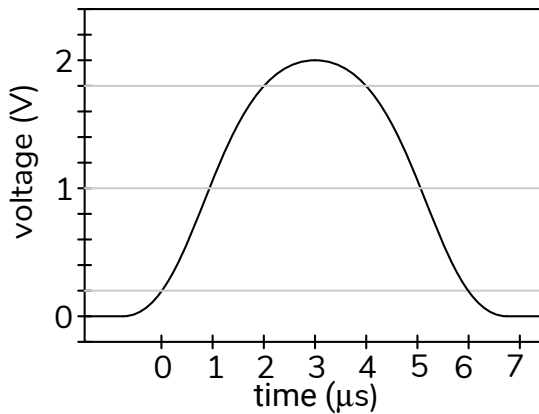
What values (in decimal) will:

(a) **a** have in module instance **f0**?

(b) **b** have in module instance **f1**?

(c) **c** have in module instance **f2**?

1. A datasheet contains the following timing diagram. **A** and **B** are inputs, **X** and **Y** are outputs. List the letters corresponding to the timing requirements that your design must meet.

2. You measure the following waveform using an oscilloscope. What are (a) the (10% to 90%) rise time of the signal, and (b) the positive pulse duration? Your answers must include units.

3. A clock divider uses a counter that counts down from $N - 1$ to zero. The clock frequency used to update the counter is 10 MHz and the divided clock frequency is 400 kHz. What is N?

4. A module is declared as:　　`module foo ( logic [15:0] a, b, c ) ;`

   Three of these modules are instantiated as follows:

   ```
   logic [15:0] a=1, b=2, c=3 ;
   foo f0 ( .* ) ;
   foo f1 ( .a(b), .b, .c(15'd4) ) ;
   foo f2 ( .b(c), .a(15'd1), .* ) ;
   ```

   What values (in decimal) will:

   (a) **c** have in module instance **f0**?

   (b) **b** have in module instance **f1**?

   (c) **a** have in module instance **f2**?