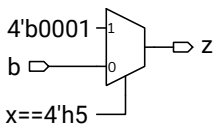
1. Write the module definition for a module named **`detect`** with a 12-bit **`logic`** input named **`level`**, a one-bit input named **`enable`** and a one-bit **`logic`** output named **`alarm`**. Multi-bit inputs should be declared with the bit indices in decreasing order.

2. Write an **`assign`** statement that sets the signal **`value_next`** to the signal **`value`** minus the signal **`decr`**.

3. Write the Verilog for a 10-bit numeric literal whose value is 8 (in decimal notation). Use a binary base for the value.

4. Write a Verilog statement corresponding to the following block diagram. Assume all signals have been declared.



1. Write the module definition for a module named **`counter`** with two single-bit **`logic`** inputs named **`reset`** and **`enable`**, and a 16-bit **`logic`** output named **`count`**. Multi-bit inputs should be declared with the bit indices in decreasing order.

2. Write an **`assign`** statement that sets the signal **`counter_next`** to the signal **`counter`** plus the signal **`incr`**.

3. Write the Verilog for a 12-bit numeric literal whose value is 16 (in decimal notation). Use a hexadecimal base for the value.

4. Write a Verilog statement corresponding to the following block diagram. Assume all signals have been declared.