ELEX 2117 : Digital Techniques 2
2021 Fall Term

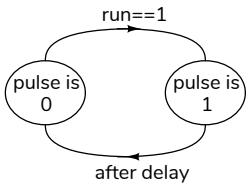
Solutions to Midterm Exam 2

Question 1

Write the a System Verilog module declared as shown below that generates a 10 (or 30) μs positive pulse after **run** is asserted. The **clk** frequency is 1 MHz. You may assume **run** is asserted for less than the duration of the output pulse.

```
module oneshot
  ( input logic run, clk,
    output logic pulse ) ;

   // your code here

endmodule
```

The state transition diagram below further describes the operation of the circuit and the waveform in Figure 1 shows the behaviour if the pulse duration were 5 μs.



You need not repeat the module declaration given but you must declare any other signals in your design. You may assume all registers have been reset to zero before **run** is asserted.

Follow the course coding conventions. You need not include comments.

Answer

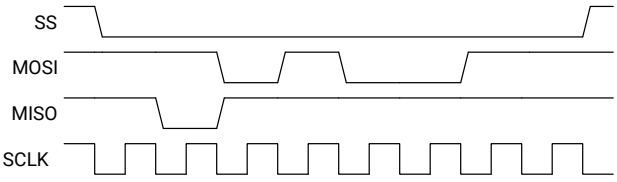
There were two version of this question with pulse durations of 10 and 30 μs.

One solution is shown below and the waveform generated is shown in Figure 2.

```
// ex49.sv
// Solution for ELEX 2117 202130 Midterm 2 Q. 1
// Ed. Casas 2021-11-11

// One-shot timer (for 10us)

module oneshot
  ( input logic run, clk,
    output logic pulse ) ;

   // counter has values N...1 on clock cycles
   // that pulse output should be asserted

   logic [3:0] count='0, count_next ;

   assign count_next
     = count ? count - 1'b1 : // is on
       run ? 4'd10 :          // start
       '0 ;                   // is off
   always_ff @(posedge clk) count = count_next ;

   // solution with (non-registered) output:
   assign pulse = count ? '1 : '0 ;

endmodule

// testbench

module oneshot_tb ;

   logic run, clk, pulse ;

   oneshot o0 ( run, clk, pulse ) ;

   initial begin
      $dumpvars ;
      clk = '0 ;
      run = '1 ;
      #2us run = '0 ;
      #10us $finish ;
   end

   always #0.5us clk = ~clk ;

endmodule
```

Question 2

You see the following waveforms on the SPI interface between a microcontroller (master) and a temperature sensor (slave):



The data is transferred most-significant bit first. What is the value that was written to (or read from) the sensor? Give your answer as a decimal number.

Answer

The value written to the sensor is transferred from the microcontroller (master) to the sensor (slave) over

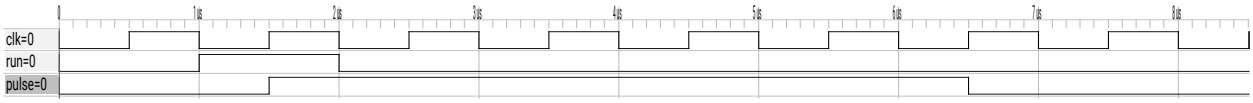


Figure 1: Example Waveforms for Question 1.

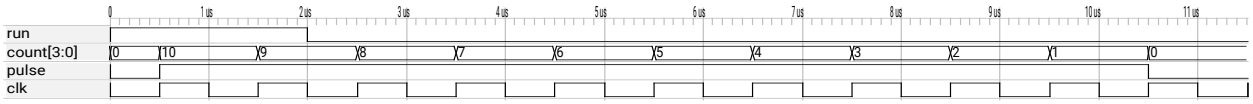
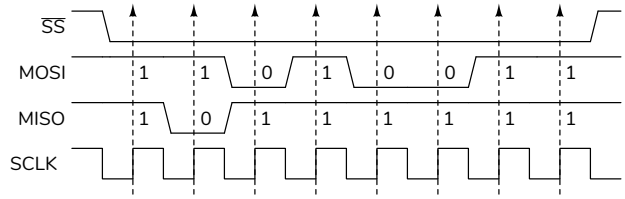


Figure 2: Waveforms for Solution to Question 1 (10 μs case).

MOSI. The bit values on MOSI are shown below. In Verilog notation the value is `8'b1101_0011` which is `0xd3` hex or 211 in decimal.



The value read from the sensor is transferred from the sensor (slave) to the microcontroller (master) over MISO. The bit values on MISO are shown above. In Verilog notation the value is `8'b1011_1111` which is `0xbf` hex or 191 in decimal.

Question 3

A logic circuit uses registers with a minimum setup time of 12 ns, a minimum hold time of 0 ns and a maximum clock-to-output delay of 2 ns. You would like the circuit to run with a clock rate of 50 (or 25) MHz. What is the maximum allowable propagation delay through any combinational logic in this design?

Answer

There were two versions of this question, one with a desired clock rate of 50 MHz (t_{clock} = 20 ns) and another with a desired clock rate of 25 MHz (t_{clock} = 40 ns). The maximum allowable propagation delay through any combinational logic is given by t_{PD} = t_{clock} - $t_{SU(required)}$ - t_{CO} = $20 - 12 - 2 = 6$ ns for a 50 MHz clock and $40 - 12 - 2 = 26$ ns for a 25 MHz clock.

Question 4

(a) How many bytes can be stored in a 16 (or 8) kByte memory? How may bits? Give your answers as decimal numbers.

(b) Does a read (or write) cycle change the contents of a DRAM?

(c) Is DRAM (or flash) memory volatile?

(d) Are SRAM and DRAM examples of mass storage technologies?

Answer

(a) A 16 kByte memory stores $16 \times 2^{10} = 16384$ bytes and $16384 \times 8 = 131,072$ bits. An 8 kByte memory stores $8 \times 2^{10} = 8192$ bytes and $8192 \times 8 = 65536$ bits.

(b) No, a read cycle does not change the contents of a memory (DRAM or any other). Yes, a write cycle can change the contents of a DRAM (or any other memory).

(c) Yes, DRAM is volatile since the contents are lost when power is removed. No, flash memory is not volatile since the contents are retained when power is removed.

(d) No, SRAM and DRAM are not examples of "mass storage" technologies, they are memory technologies.