ELEX 2117 : Digital Techniques 2
2021 Fall Term

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MIDTERM EXAM 2
15:30 – 17:20
Friday, November 12, 2021
SW01-1025

This exam has four (4) questions on four (4) pages. The marks for each question are as indicated. There are a total of eighteen (18) marks. Answer all questions. Write your answers and all rough work in this paper *and nowhere else*. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

You may not leave the exam room before 4:30 PM.

This exam paper is for:

Sample Exam 1 A00000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		6
2		4
3		3
4		5
Total		18

Question 1 — 6 marks

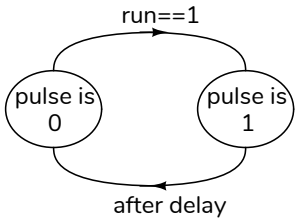
Write the a System Verilog module declared as shown on the right that generates a 30 μs positive pulse after **run** is asserted. The **clk** frequency is 1 MHz. You may assume **run** is asserted for less than the duration of the output pulse.

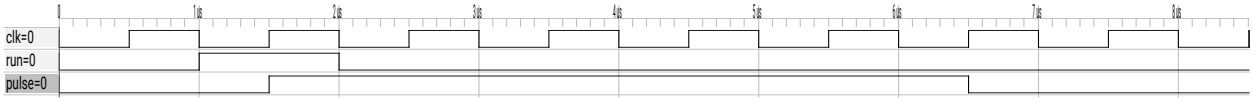
The state transition diagram on the right further describes the operation of the circuit and the waveform below shows the behaviour if the pulse duration were 5 μs.

You need not repeat the module declaration given but you must declare any other signals in your design. You may assume all registers have been reset to zero before **run** is asserted.

Follow the course coding conventions. You need not include comments.

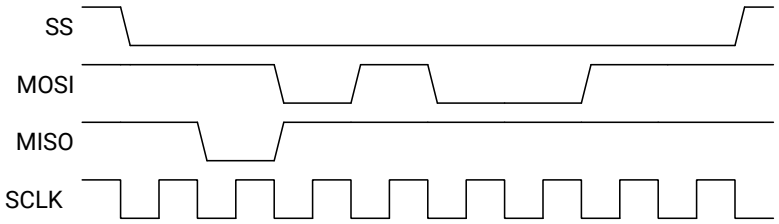
```
module oneshot
  ( input logic run, clk,
    output logic pulse ) ;

   // your code here

endmodule
```





Question 2 — 4 marks

You see the following waveforms on the SPI interface between a microcontroller (master) and a temperature sensor (slave):



The data is transferred most-significant bit first. What is the value that was read from the sensor? Give your answer as a decimal number.

Question 3 — 3 marks

A logic circuit uses registers with a minimum setup time of 12 ns, a minimum hold time of 0 ns and a maximum clock-to-output delay of 2 ns. You would like the circuit to run with a clock rate of 25 MHz. What is the maximum allowable propagation delay through any combinational logic in this design?

Question 4 — 5 marks

(a) How many bytes can be stored in a 8 kByte memory? How may bits? Give your answers as decimal numbers.

(b) Does a write cycle change the contents of a DRAM?

(c) Is flash memory volatile?

(d) Are SRAM and DRAM examples of mass storage technologies?

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Question	Mark	Max.
1		6
2		4
3		3
4		5
Total		18

Question 1 — 6 marks

Write the a System Verilog module declared as shown on the right that generates a 10 μs positive pulse after **run** is asserted. The **clk** frequency is 1 MHz. You may assume **run** is asserted for less than the duration of the output pulse.

The state transition diagram on the right further describes the operation of the circuit and the waveform below shows the behaviour if the pulse duration were 5 μs.

You need not repeat the module declaration given but you must declare any other signals in your design. You may assume all registers have been reset to zero before **run** is asserted.

Follow the course coding conventions. You need not include comments.

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  ( input logic run, clk,
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endmodule
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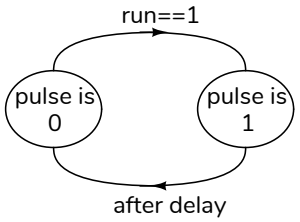
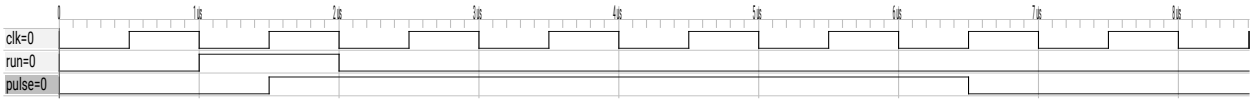
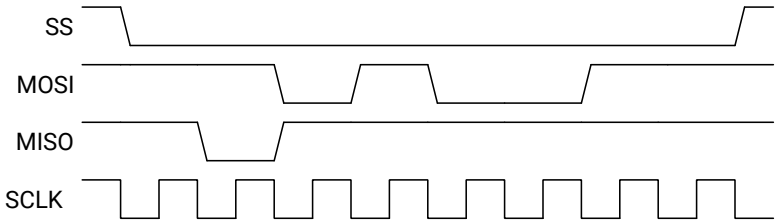




Question 2 — 4 marks

You see the following waveforms on the SPI interface between a microcontroller (master) and a temperature sensor (slave):



The data is transferred most-significant bit first. What is the value that was written to the sensor? Give your answer as a decimal number.

Question 3 — 3 marks

A logic circuit uses registers with a minimum setup time of 12 ns, a minimum hold time of 0 ns and a maximum clock-to-output delay of 2 ns. You would like the circuit to run with a clock rate of 50 MHz. What is the maximum allowable propagation delay through any combinational logic in this design?

Question 4 — 5 marks

(a) How many bytes can be stored in a 16 kByte memory? How may bits? Give your answers as decimal numbers.

(b) Does a read cycle change the contents of a DRAM?

(c) Is DRAM memory volatile?

(d) Are SRAM and DRAM examples of mass storage technologies?