ELEX 2117 : Digital Techniques 2
2021 Fall Term

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MIDTERM EXAM 1
15:30 – 17:20
Friday, October 8, 2019
SW01-1025

This exam has seven (7) questions on eight (8) pages. The marks for each question are as indicated. There are a total of forty (40) marks. Answer all questions. Write your answers and all rough work in this paper *and nowhere else*. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

This exam paper is for:

Sample Exam 1 A00000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		6
2		5
3		5
4		6
5		6
6		9
7		3
Total		40

Question 1 — 6 marks

Fill in the blank boxes in the table below so that all of the columns in each row match. Give the value using decimal base (base 10).

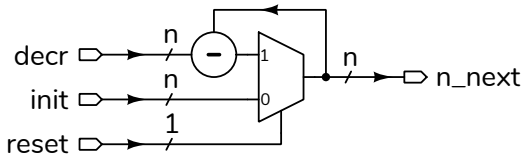
bit width (bits)	base	value (decimal)	Verilog literal
`19`	`decimal (10)`	`9`	
			`8'b100`
`12`	`hex (16)`	`17`	
			`8'h15`

Question 2 — 5 marks

Write the module definition for a module named **`dac`** with a 10-bit **`logic`** input named **`val`**, a one-bit **`logic`** input named **`sclk`** and a one-bit **`logic`** output named **`err`**. Multi-bit signals should be declared with the bit indices in decreasing order.

Question 3 — 5 marks

Write one Verilog **`assign`** statement that implements the following schematic. Do not include any **`module`** or signal declarations or other statements. Assume all signals have been declared and have the proper widths.



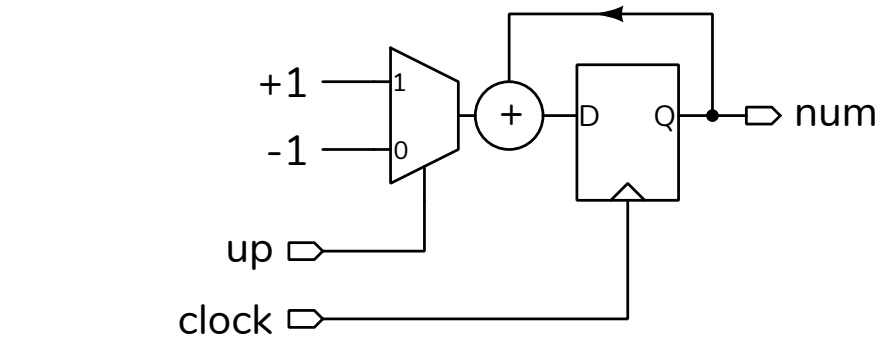
Question 4 — 6 marks

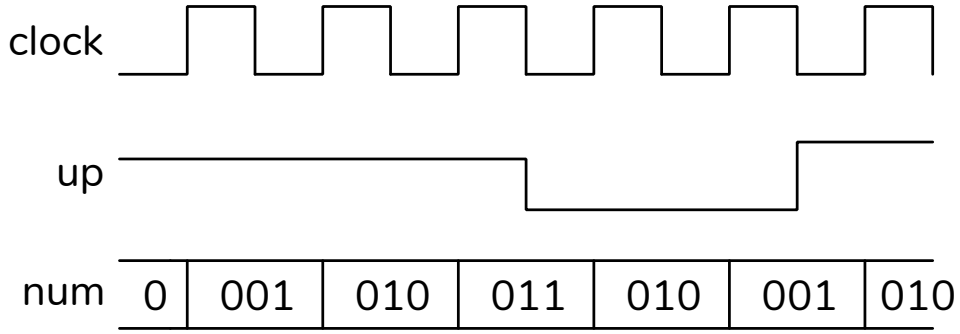
Fill in the blank boxes in the table below so that all values in each row are consistent. The first row is an example.

signal name	truth value (T/F)	logic level (H/L)	Verilog value (0/1)
`on`	T	H	1
`closed*`		L	
`open`		L	
$\overline{\texttt{on}}$			1

Question 5 — 6 marks

The following schematic shows a 3-bit register whose value, **`val`** can go up or down by 1 under control of an **`up`** input.





The initial value of the register is zero.

Fill in the **`val`** waveform. Draw a vertical line between the dashed lines where the output's value changes. Write the output's value as a binary number in-between each change. For example:

Question 6 — 9 marks

A Verilog module implementing a state machine is declared as follows:

```
module bitshrink
(
   input logic clock, reset, enable,
   output logic [2:0] bits
) ;
   // ... your code goes here ...
endmodule
```

The **bits** output changes on the rising edge of **clock** – a periodic clock input. The **bits** output can be **3'b000**, **3'b001**, **3'b011**, or **3'b111**. The **reset** and **enable** inputs control the state machine as follows:

- if reset is asserted (H), the output is set to **3'b111**,
- otherwise, if enable is not asserted (L), the output doesn't change,
- otherwise, if enable is asserted (H) then the value with one less bit set to **1** is output unless the output is already **3'b000**; in this case the output doesn't change.

(a) Draw the state transition diagram. Label each state with the corresponding value of **bits**. Unambiguously label the state transitions with the values of **reset** and **enable** required for that transition. You need not include transitions that do not result in a change of state.

(b) Write the rest of the Verilog code required to implement this state machine. Only write the part between the comment and **`endmodule`**. Include any necessary signal declarations. Follow the course coding conventions.

Question 7 — 3 marks

Given the following Verilog signal declarations and initial values:

```
logic x[7:0] = 8'h14 ;
logic y[3:0] = 4'd1 ;
```

fill in the following table showing the length (in bits) and values (in binary) of each of the following expressions:

expression	length (bits)	value (binary)
`x + y`		
`x << 4'b2`		
`x[3:0]`		
`{x,y}`		

255

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Question 1 — 6 marks

Fill in the blank boxes in the table below so that all of the columns in each row match. Give the value using decimal base (base 10).

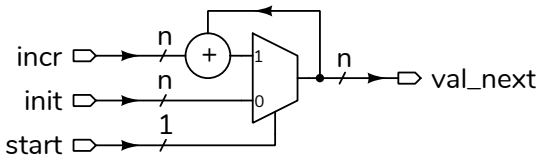
bit width (bits)	base	value (decimal)	Verilog literal
`9`	`decimal (10)`	`19`	
			`8'b100`
`16`	`hex (16)`	`17`	
			`8'h14`

Question 2 — 5 marks

Write the module definition for a module named **`uart`** with two single-bit **`logic`** inputs named **`clock`** and **`sin`**, and an 8-bit **`logic`** output named **`data`**. Multi-bit signals should be declared with the bit indices in decreasing order.

Question 3 — 5 marks

Write one Verilog **`assign`** statement that implements the following schematic. Do not include any **`module`** or signal declarations or other statements. Assume all signals have been declared and have the proper widths.



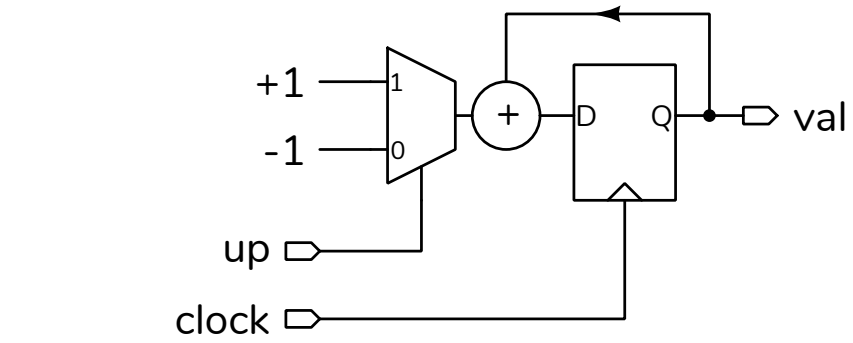
Question 4 — 6 marks

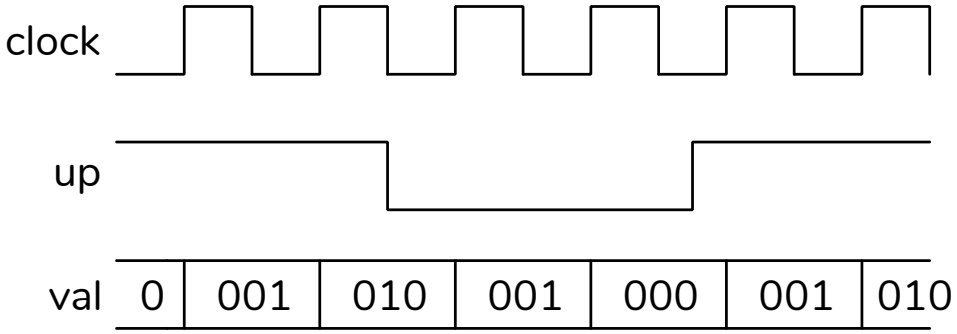
Fill in the blank boxes in the table below so that all values in each row are consistent. The first row is an example.

signal name	truth value (T/F)	logic level (H/L)	Verilog value (0/1)
`off`	**`T`**	**`H`**	**`1`**
`open*`		**`L`**	
`closed`		**`L`**	
$\overline{\texttt{off}}$			**`1`**

Question 5 — 6 marks

The following schematic shows a 3-bit register whose value, **num** can go up or down by 1 under control of an **up** input.





The initial value of the register is zero.

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```
module bitshrink
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   input logic clock, reset, enable,
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The `bits` output changes on the rising edge of `clock` – a periodic clock input. The `bits` output can be `3'b000`, `3'b001`, `3'b011`, or `3'b111`. The `reset` and `enable` inputs control the state machine as follows:

- if reset is asserted (H), the output is set to `3'b000`,
- otherwise, if enable is not asserted (L), the output doesn't change,
- otherwise, if enable is asserted (H) then the value with one more bit set to `1` is output unless the output is already `3'b111`; in this case the output doesn't change.

(a) Draw the state transition diagram. Label each state with the corresponding value of `bits`. Unambiguously label the state transitions with the values of `reset` and `enable` required for that transition. You need not include transitions that do not result in a change of state.

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Question 7 — 3 marks

Given the following Verilog signal declarations and initial values:

```
logic x[7:0] = 8'h12 ;
logic y[3:0] = 4'd2 ;
```

fill in the following table showing the length (in bits) and values (in binary) of each of the following expressions:

expression	length (bits)	value (binary)
`x + y`		
`x << 4'b2`		
`x[3:0]`		
`{x,y}`		