Timing Analysis

Exercise 1: Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

T_{clock} NO

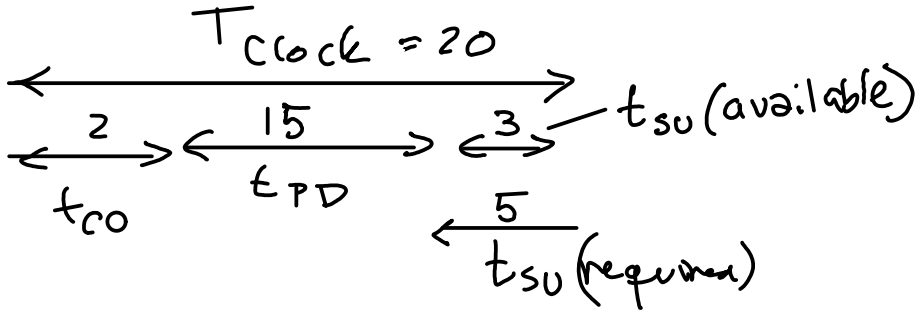
t_{CO} YES

t_{PD} YES

t_{su} (required) YES

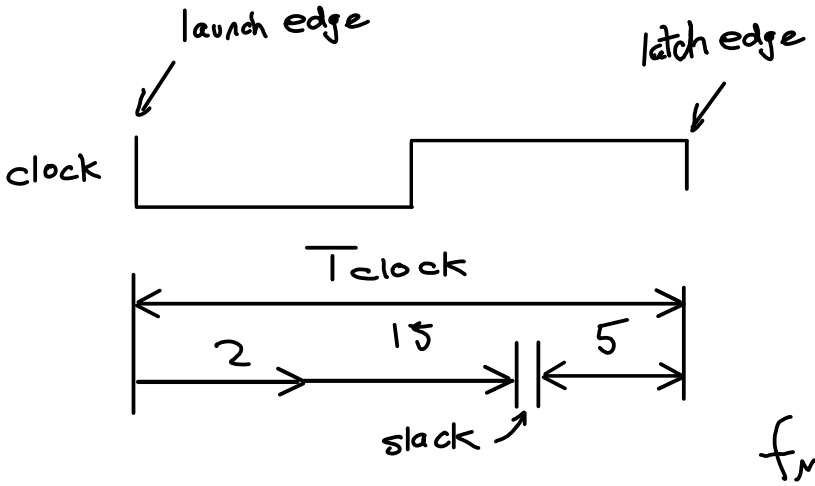
Exercise 2: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

$$T_{clock} = \frac{1}{f_{clock}} = \frac{1}{50 \times 10^6} = 20 \text{ ns}$$



slack = 3 − 5 = −2

t_{su} (reqd) not met.

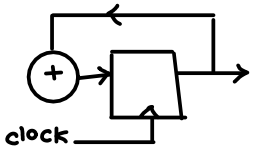


$T_{clock(min)} = 2 + 15 + 5$
$= 22\,ns$

$f_{max} = 45.45\ MHz$

clock-to-output delay

Exercise 3: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps ~~hold times~~ and adder logic that has a 250 ps propagation delay?

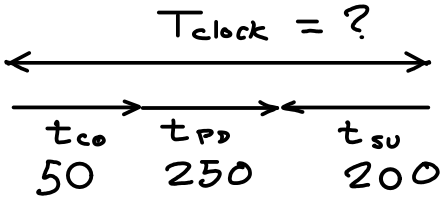


$t_{su(avail.)} = T_{clock} - t_{PD} - t_{co}$

$t_{su(reqd.)} = 200ps$

$t_{co} = 50ps$

$t_{PD} = 250$



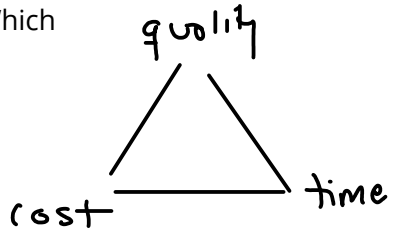
$T_{clock(min)} = t_{su}^{(reqd)} + t_{PD} + t_{co}$

$= 200 + 250 + 50$

$= 500ps$

$f_{clock(max)} = \frac{1}{500ps} = 2\ GHz.$

Exercise 4: Which of the above would increase design time? Which would increase the unit costs? Which would lower quality?



time - redesign

cost - faster ports

quality - reduce f_{max} required.