Flip-Flops and Registers

Exercise 1: Is a signal named **overload** active-high or active-low? Is there an overload if this signal is high? What if the signal was named **overload**?

anything is active-low

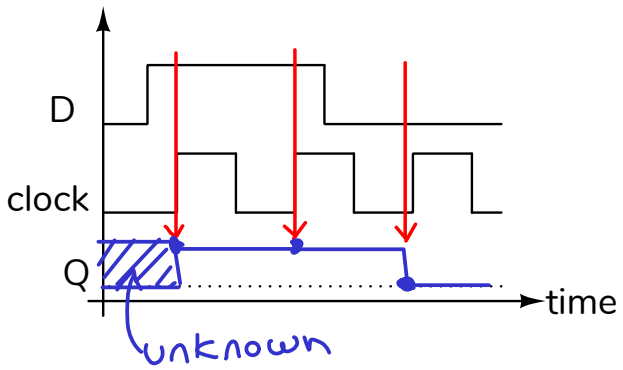
active low → L is true
H is false → overload is false

overload is active-high → H is true → overload is true
L is false

Exercise 2: Come up with an appropriate name for a signal that is at 3 V when a door is open and 0 V when the door is closed.

3 V = H → true → open
0 V = L

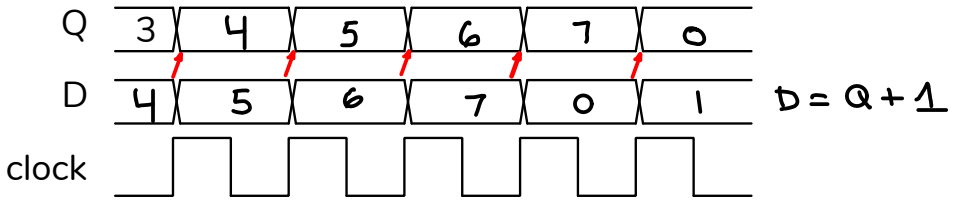
Exercise 3: Fill in the waveform for the Q signal in the diagram above.



Exercise 4: What would be another name for a 1-bit register?

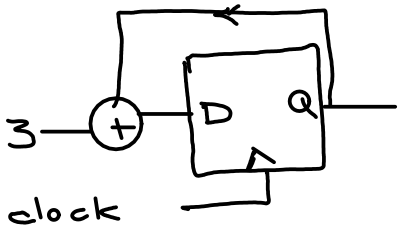
a flip-flop

Exercise 5: Assuming a 3-bit counter, fill in the values of D and Q in the diagram above.

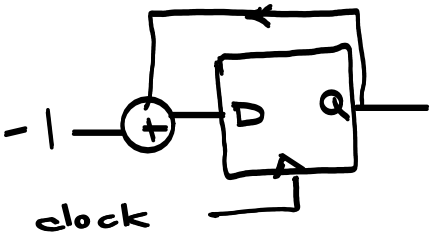


Exercise 6: Draw the block diagram for a counter that: (a) counts up by 3? (b) counts down by 1? (c) whose value doubles on each clock edge?

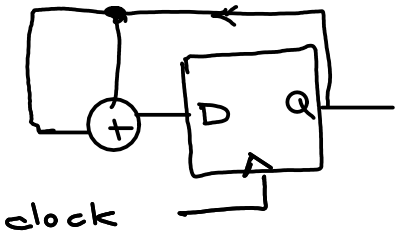
(a)



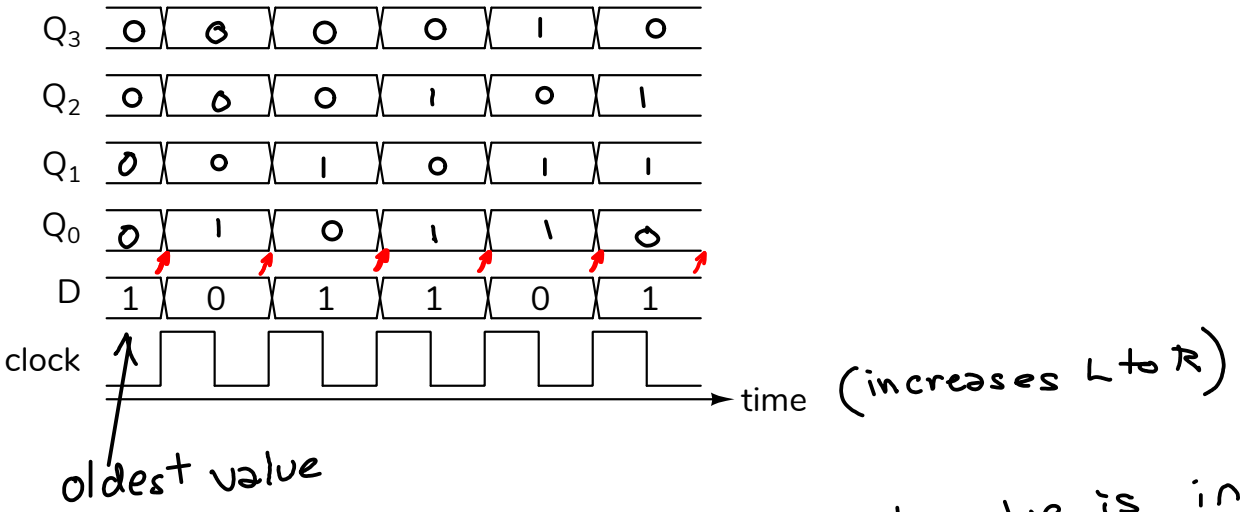
(b)

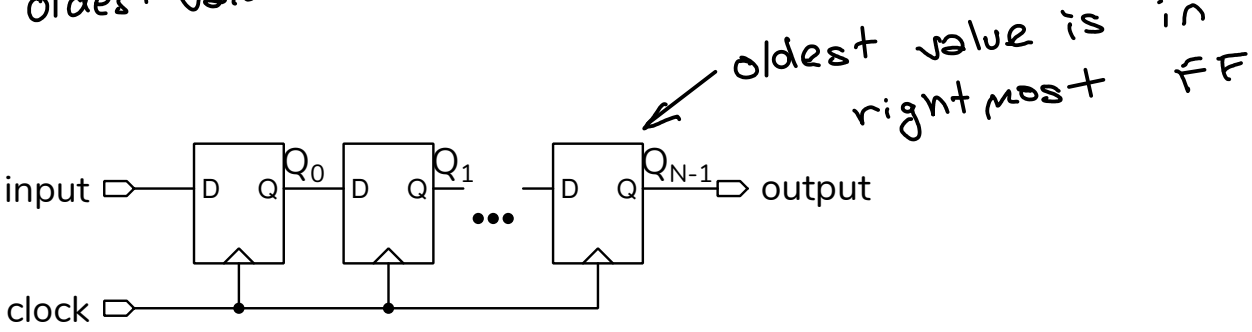


(c)



Exercise 7: Fill in the diagram above for a 4-bit shift register. Assume the initial value of each flip-flop is zero. Which is the oldest (first) value the D waveform? Which flip-flop holds the oldest value?

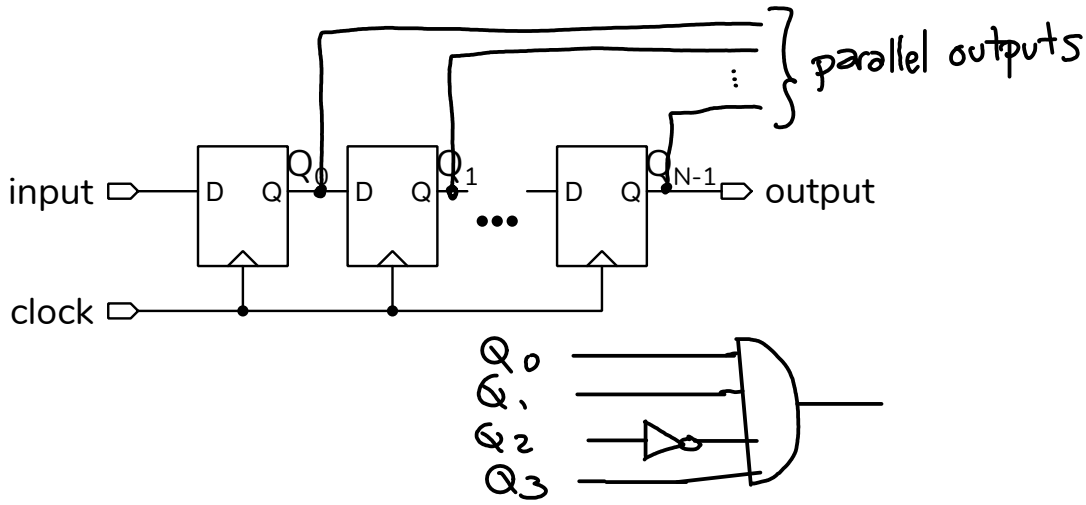


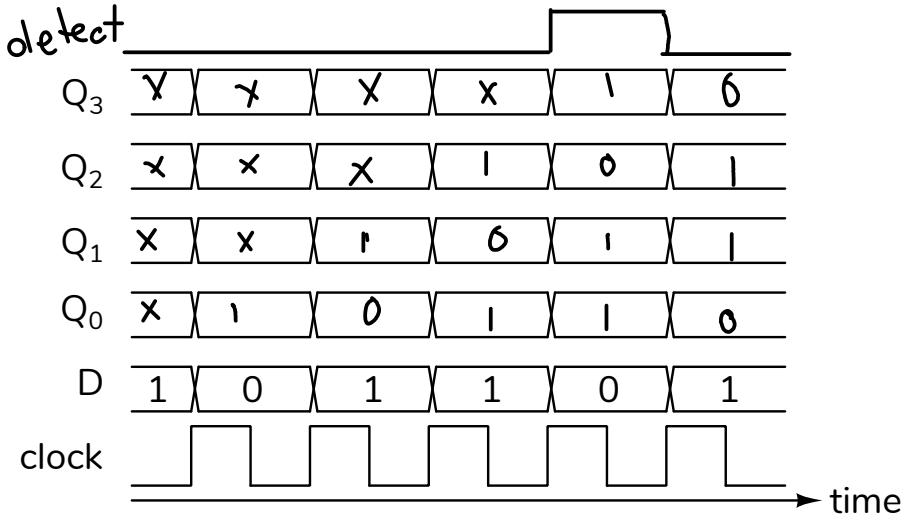


$X = y - 1$

$X <= y + 1$

Exercise 8: Add parallel outputs to the shift register schematic. Draw a circuit whose output is high when the sequence 1, 0, 1, 1 is detected. Add the output of this circuit to the timing diagram above.





Exercise 9: What would you change to make an 8-bit register? A 4-bit counter? A 3-bit shift register? Follow the course coding conventions.

```
module ex2 (input logic d, clk,
            output logic q) ;

   always_ff @(posedge clk)
     q <= d ;

endmodule
```

8-bit register

8-bit register:

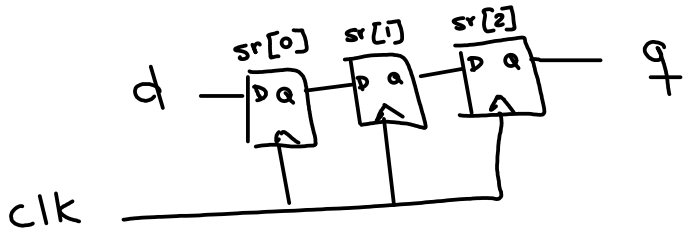
d[7:0]
q[7:0]

4-bit counter:

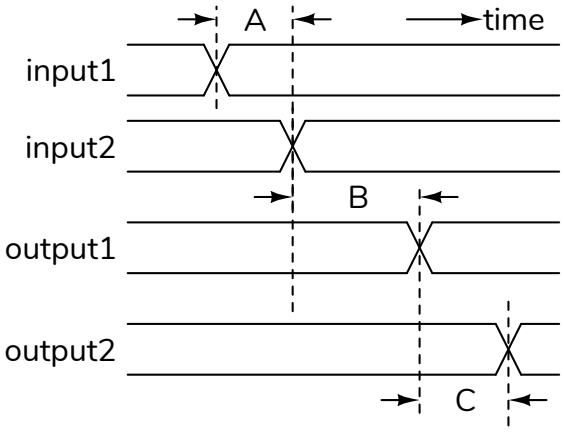
~~d~~ → no input
q[3:0]
q = q + 1;

3-bit shift register:

logic sr[2:0];
always_ff ...
sr = {sr[1:0], d};
assign q = sr[2];



Exercise 10: Label the specifications A through C as requirements or guaranteed responses.



A: to input: requirement

B: to output: guaranteed

C: to outpot: guaranteed