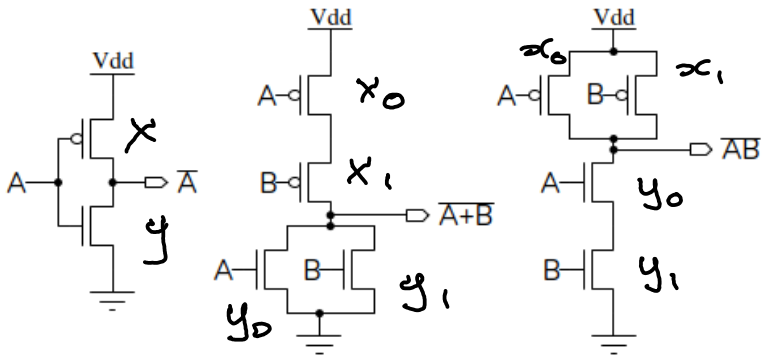
Implementation of Digital Logic Circuits

Exercise 1: Which transistors are on when the output is high? When it is low? In which direction does the output current flow in each case?



HIGH OUT: ON: x, OFF: y

ON: x_0 AND x_1
OFF: y_0 AND y_1

ON: x_0 OR x_1
OFF: y_0 OR y_1

LOW OUT: ON: y, OFF: x

ON: y_0 OR y_1
OFF: x_0 OR x_1

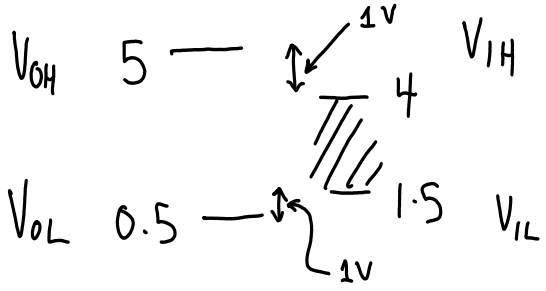
ON: y_0 AND y_1
OFF: x_0 AND x_1

Exercise 2: Which of these specifications does the manufacturer guarantee? Which are requirements?

guaranteed: outputs (V_{OL}, V_{OH})

requirements: inputs (V_{IL}, V_{IH})

Exercise 3: A logic family has ~~V_{OH}~~.(min) = 5 V, ~~V_{OL}~~.(max) = 0.5 V, ~~V_{IH}~~.(min) = 4 V ~~V_{IL}~~ = 1.5 V. What are the noise margins?

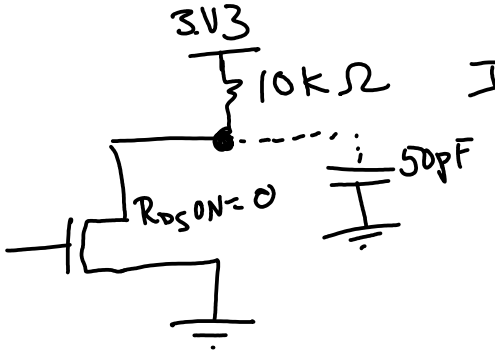


Exercise 4: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

frequency: reduce power by 50x (increase by $\frac{1}{50}$)

voltage: $\frac{3.3^2}{5^2} \approx \frac{10}{25} \approx 44\%$ of power at 5V.

Exercise 5: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?



$I = \frac{V}{R} = \frac{3.3}{10k} = 0.33\,mA = 330\,\mu A.$

$RC = 10k \cdot 50 \times 10^{-12} = 500 \times 10^{-9}$

$= 0.5\,\mu s.$

Exercise 6: How many square mm of PCB area does each package require? Which packages have their pins accessible when the packages is placed on the PCB?

TQFP: $22^2\ mm^2 \approx 400\ mm^2$ (pins accessible)

BGA: $3.5^2 \approx 10\ mm^2$ (pins not accessible)