## Introduction to Digital Design with Verilog HDL

**Exercise 1**: What changes would result in a 3-input OR gate?

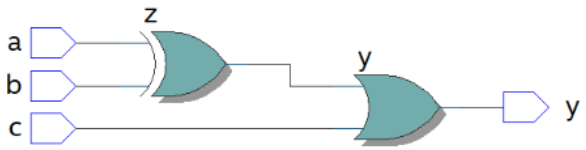
```
// AND gate in Verilog

module ex1 ( input logic a, b, c,
             output logic y ) ;

  assign y = a | b |c ;

endmodule
```

**Exercise 2**: What schematic would you expect if the statement was `assign y = ( a ^ b ) | c ;`?




**Exercise 3**: If the signal `i` is declared as `logic [2:0] i;`, what is the 'width' of `i`? If `i` has the value 6 (decimal), what is the value of `i[2]`? Of `i[0]`?

2:0 is 3 bits wide (indices 2, 1, 0)

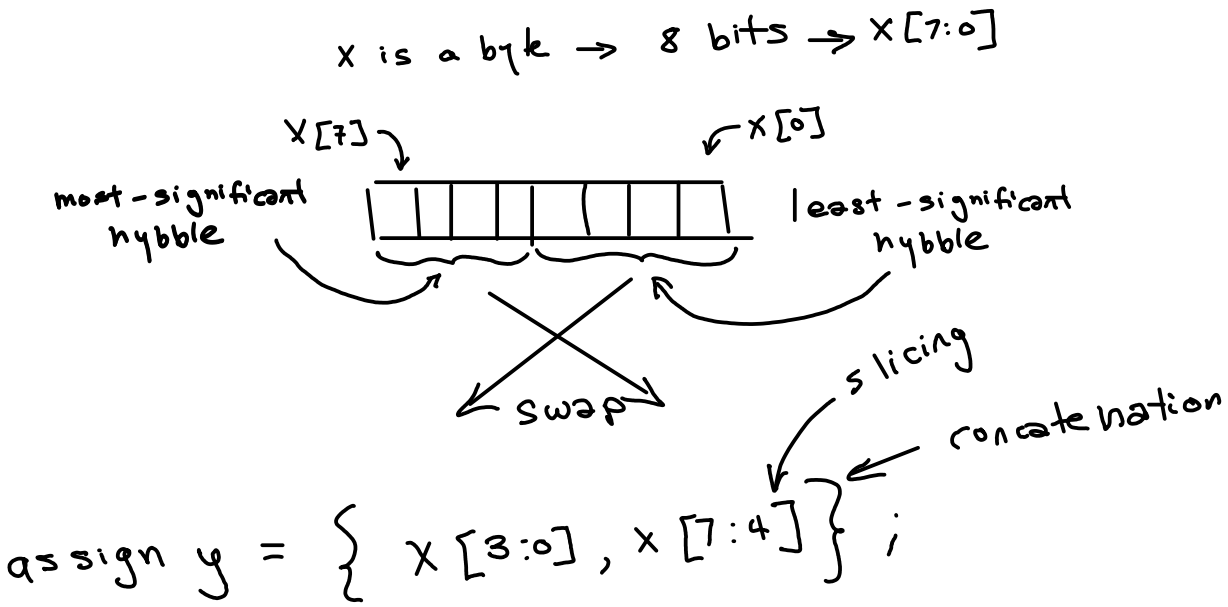
6 in binary would be 110

i[2] i[1] i[0]

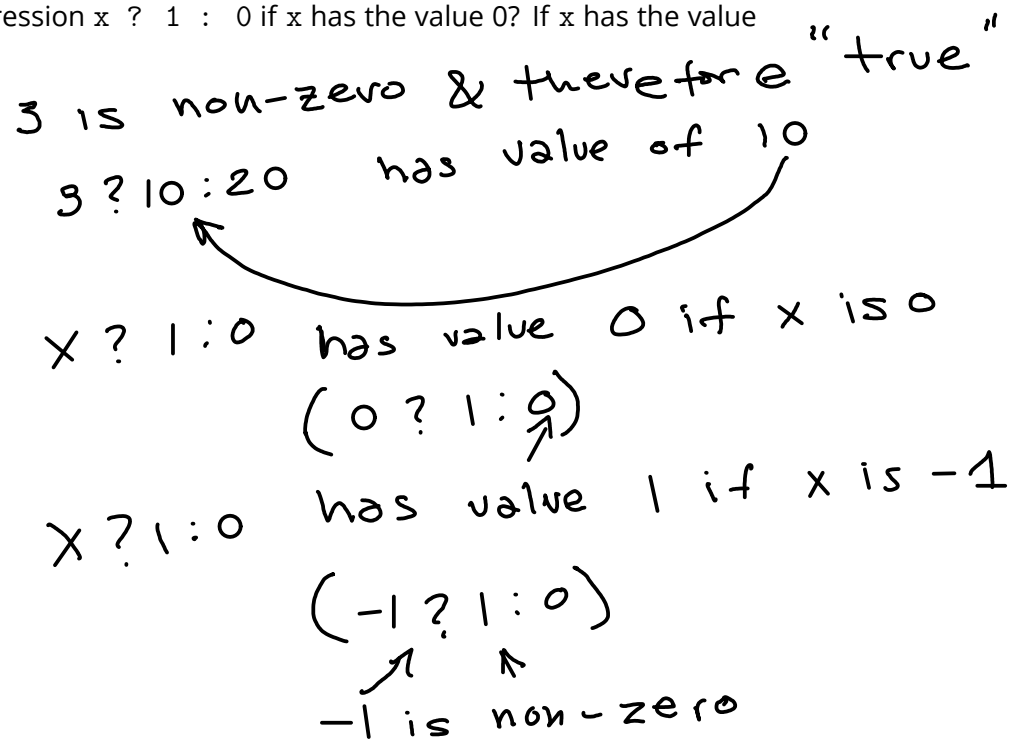
∴ i[2] = 1

i[0] = 0

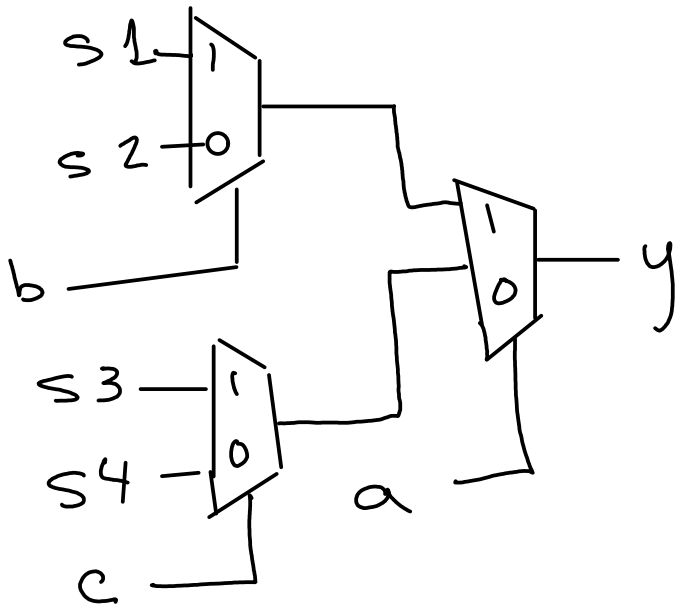
**Exercise 4**: Use slicing and concatenation to assign `y` the value of the byte `x` with its nybbles swapped.




**Exercise 5**: What is the value of the expression `3 ? 10 : 20`? Of the expression `x ? 1 : 0` if `x` has the value 0? If `x` has the value -1?



**Exercise 6**: Draw the schematic corresponding to: `y = a ? ( b ? s1 : s2 ) : ( c ? s3 : s4 )`




**Exercise 7**: Write a Verilog description of a 4-bit 3-to-1 multiplexer controlled by a 2-bit `sel` input? Label the inputs `a` (for `sel=00`) through `c` (for `sel=10`).

```
assign y = sel == 2'b00 ? a :
           sel == 2'b01 ? b :
           sel == 2'b10 ? c : ??? ;
```

output for sel == 2'b11 not defined in the question.

**Exercise 8**: What are the sizes and values, in decimal, of the following: 4'b1001, 5'd3, 6'h0_a, 3?

| | width | value |
|---|---|---|
| 4'b1001 | 4 | $1001_2 = 9_{10}$ |
| 5'd3 | 5 | $3_{10} = 3$ |
| 6'h0_a | 6 | $0A_{16} = 10_{10}$ |
| 3 | 32 (default) | $3_{10} = 3$ |