ELEX 2117 : Digital Techniques 2
2021 Fall Term

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FINAL EXAM
14:30 – 17:30
Tuesday, December 7, 2021
SW09-110

This exam has eleven (11) questions on six (6) pages. The marks for each question are as indicated. There are a total of twenty-seven (27) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		3
2		2
3		1
4		2
5		4
6		2
7		4
8		1
9		5
10		1
11		2
Total		27

Question 1 — 3 marks

Given the following Verilog code:

```
module ex50
  ( input logic reset, clock,
    output logic [3:0] count ) ;

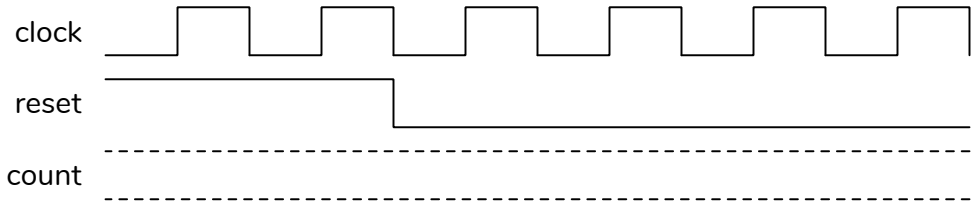
   logic [3:0] count_next ;

   assign count_next
     = reset ? 4'd1 :
       count + 4'd2 ;

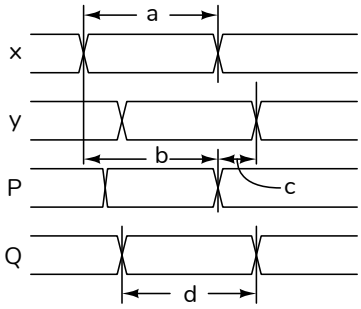
   always_ff @(posedge clock) count = count_next ;

endmodule
```

and the input signals in the diagram below, draw a vertical line between the dashed lines where the **count** output changes and write the value of **count** in-between each vertical line. Write an **X** if the value is undefined.



Question 2 — 2 marks



In the timing diagram above **x** and **y** are outputs, **P** and **Q** are inputs, and **a** through **d** are timing specifications. Write the letters corresponding to the timing specifications that are timing requirements and guaranteed responses in the appropriate boxes below. Each box should have zero or more of the letters **a** through **d**.

timing requirements	guaranteed responses

Question 3 — 1 marks

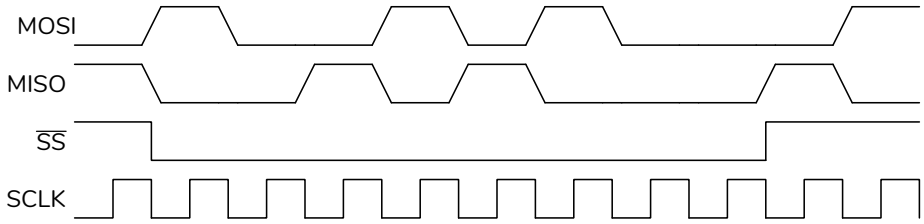
Given the following Verilog declarations:

```
logic [3:0] x = 4'b0101 ;
logic [7:0] y = 8'h4e ;
```

fill in in the table below with the value of the each expression in hexadecimal and the width (number of bits) in decimal:

expression	value (hexadecimal)	width (bits, decimal)
{x,y}		
y[5:2]		
x+5'b1		
y>>2		

Question 4 — 2 marks



The waveform above is measured on an SPI interface. What value was transferred from the master to the slave? Give your answer as a hexadecimal number. Assume the bits are transferred most-significant-bit first.

Question 5 — 4 marks

A module with inputs **`reset`** and **`run`**, and a clock signal, **`clock`**, is declared as:

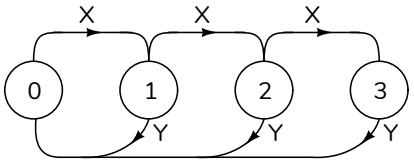
```
module statemachine
  ( input logic reset, run, clock ) ;

   logic [1:0] state, state_next ;

   // your code here

endmodule
```

The module's behaviour can be described as a state machine with four states that have values 0 through 3. The state transitions are as described in the state transition diagram below:



X: reset==0 && run==1

Y: reset==1

Write Verilog statements below that, if placed after the comment, would result in the behaviour described in the state transition diagram above. Do not repeat code already given. Follow the course coding conventions.

Question 6 — 2 marks

The maximum propagation delay through any combinational logic path in a CPLD is 18 ns, the minimum setup time of its registers is 1.5 ns and the maximum clock-to-output delay is 0.5 ns. What is the fastest clock frequency at which this CPLD can operate?

Question 7 — 4 marks

You need to design a 1 MByte memory for a 16-bit CPU using 256 k × 4 memory ICs.

(a) How many IC's will be needed?

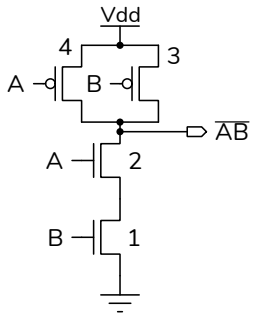
(b) How many banks will this memory require?

(c) How many address bits does each memory IC have?

(d) If an address decoder places the first byte of this memory at address **`0x10 0000`**, what is the last address in this 1 MByte memory?

Question 8 — 1 marks

The schematic below shows a CMOS NAND gate with the four transistor numbered from 1 to 4. Which transistors are on (conducting) when the output is low? You answer should be between zero and four digits. Both **`A`** inputs are at the same logic level. Both **`B`** inputs are at the same logic level.



Question 9 — 5 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

totem pole	
PLD	
RAM	
DIP	
open-collector	

(1) through-hole

(2) FPGA

(3) pull-up

(4) CMOS

(5) volatile

Question 10 — 1 marks

A logic signal interface has an output low logic level of $V_{OL(max)}$ of 0.5 V and a $V_{IL(max)}$ of 1.5 V. What is the noise margin for low logic levels?

Question 11 — 2 marks

A CMOS digital logic circuit is operating with a supply voltage of 5 V at a clock frequency of 5 MHz. You want to reduce the power consumption of this circuit by a factor of 10 (i.e. by 90%).

(i) If you were to change only the clock frequency, what frequency would you need to use?

(ii) If you were to change only the supply voltage, what voltage would you need to use?

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   logic [3:0] count_next ;

   assign count_next
     = reset ? 4'd2 :
       count + 4'd1 ;

   always_ff @(posedge clock) count = count_next ;

endmodule
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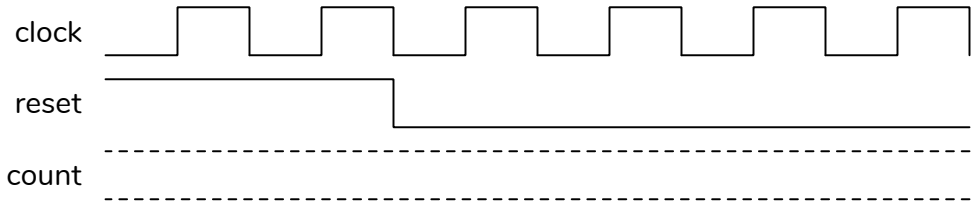
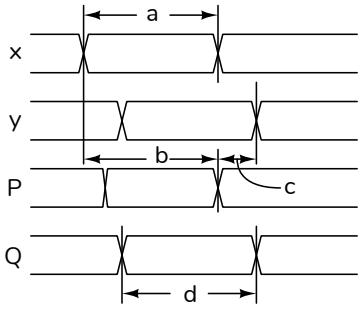


Question 2 — 2 marks



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timing requirements	guaranteed responses

Question 3 — 1 marks

Given the following Verilog declarations:

```
logic [3:0] x = 4'b1010 ;
logic [7:0] y = 8'h5e ;
```

fill in in the table below with the value of the each expression in hexadecimal and the width (number of bits) in decimal:

expression	value (hexadecimal)	width (bits, decimal)
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y[5:2]		
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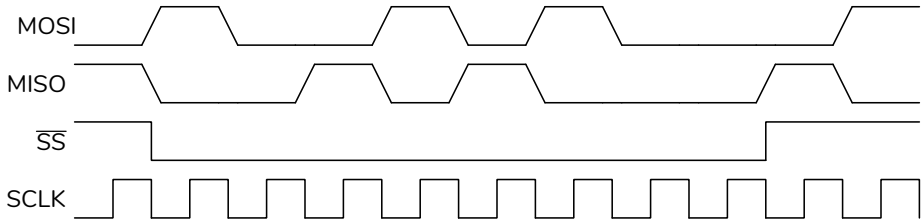

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A module with inputs **`reset`** and **`run`**, and a clock signal, **`clock`**, is declared as:

```
module statemachine
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   logic [1:0] state, state_next ;

   // your code here

endmodule
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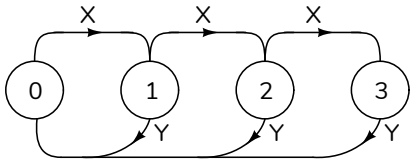

X: reset==0 && run==1

Y: reset==1

Write Verilog statements below that, if placed after the comment, would result in the behaviour described in the state transition diagram above. Do not repeat code already given. Follow the course coding conventions.

Question 6 — 2 marks

The maximum propagation delay through any combinational logic path in a CPLD is 8 ns, the minimum setup time of its registers is 1.5 ns and the maximum clock-to-output delay is 0.5 ns. What is the fastest clock frequency at which this CPLD can operate?

Question 7 — 4 marks

You need to design a 1 MByte memory for a 16-bit CPU using 256 k × 4 memory ICs.

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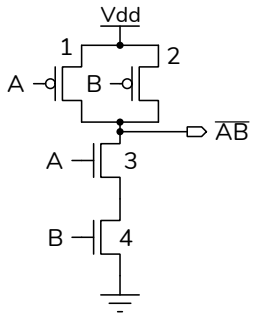

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PLD	
RAM	
DIP	
open-collector	

(1) FPGA

(2) through-hole

(3) volatile

(4) pull-up

(5) CMOS

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A logic signal interface has an output low logic level of $V_{OL(max)}$ of 0.7 V and a $V_{IL(max)}$ of 1.4 V. What is the noise margin for low logic levels?

Question 11 — 2 marks

A CMOS digital logic circuit is operating with a supply voltage of 5 V at a clock frequency of 10 MHz. You want to reduce the power consumption of this circuit by a factor of 10 (i.e. by 90%).

(i) If you were to change only the clock frequency, what frequency would you need to use?

(ii) If you were to change only the supply voltage, what voltage would you need to use?