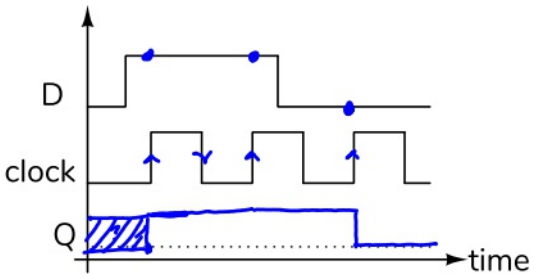
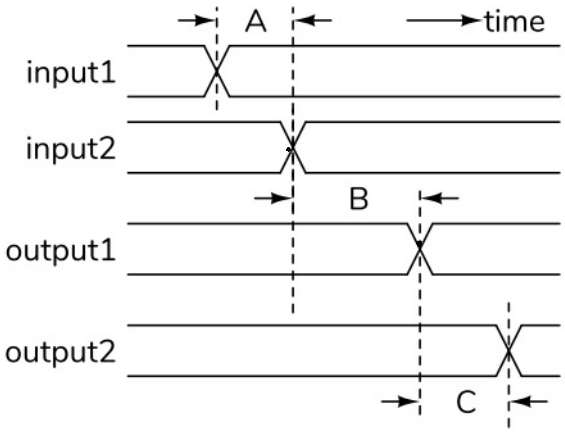
Flip-Flops and Registers

Exercise 1: Fill in the waveform for the Q signal in the diagram above.



Exercise 2: Label the specifications A through C as requirements or guaranteed responses.



A: requirement

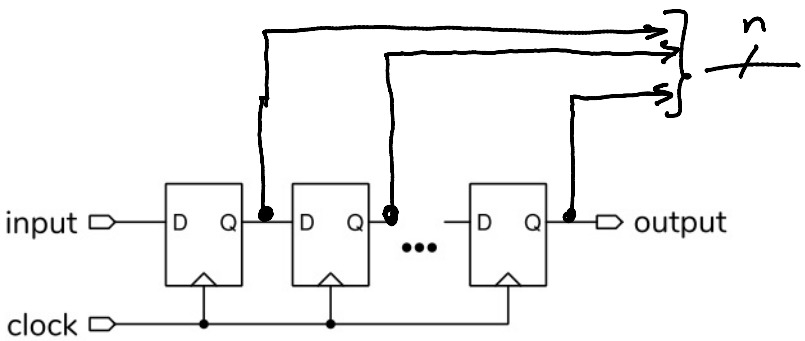
B: guaranteed

C: guaranteed.

Exercise 3: What would be another name for a 1-bit register?

D Flip-flop

Exercise 4: Add the parallel outputs to the shift register diagram.



Exercise 5: What would you change to make an 8-bit register? A 3-bit (deep) shift register? A 4-bit counter?

4-bit counter (w/ reset)

```
1  module ex2 (input logic reset, clk,
2              output logic q[3:0] ) ;
3
4     logic [3:0] q_next ;
5
6     always_ff @(posedge clk)
7        q <= q_next ;
8
9     assign q_next = reset ? 0 : q + 1 ;
10
11 endmodule
```