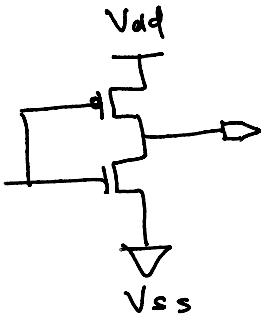
Implementation of Digital Logic Circuits

Exercise 1: If $\overline{D}$ is a data bus and $\overline{D0}$ is low, is the value on the data bus an even or odd number?

$\overline{D0}$ is the least-significant bit and Low = 1

. it's an odd number.

Exercise 2: Which transistors are on when the output is high? When it is low? In which direction does the output current flow in each case?



	high	low
	ON	OFF
	OFF	ON
	OUT	IN ← current

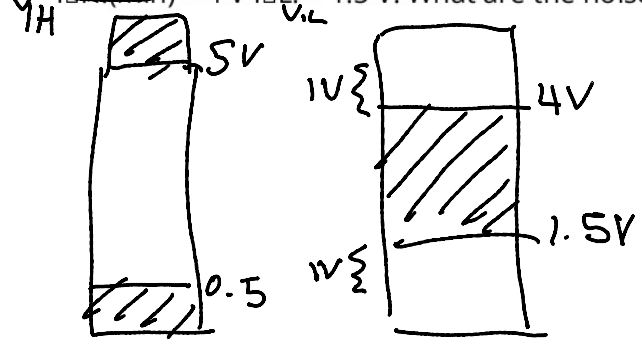
Exercise 3: Which of these specifications does the manufacturer guarantee? Which are requirements?

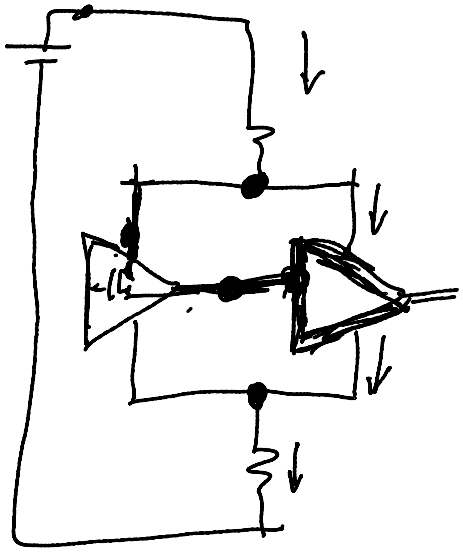
were not defined for voltage levels

V_{OH}, V_{OL} } guaranteed

V_{IL}, V_{IH} } required

Exercise 4: A logic family has V_{OH}(min) = 5 V, V_{OL}(max) = 0.5 V, V_{IH}(min) = 4 V, V_{IL} = 1.5 V. What are the noise margins?



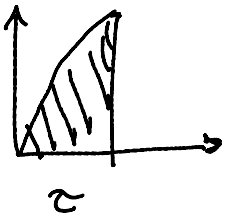


noise margin (H) = $5 - 4 = 1$ V

noise margin (L) = $1.5 - 0.5$ V

} typically quote as positive number.

Exercise 5: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?



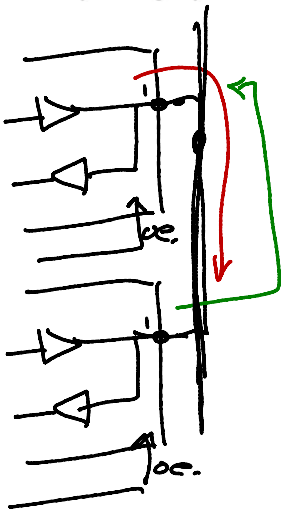
power = $c f v^2$

$$\frac{P_{3.3}}{P_5} = \frac{c \cdot f \cdot (3.3)^2}{c \cdot f \cdot 5^2} = \frac{11}{25} < \frac{1}{2}$$

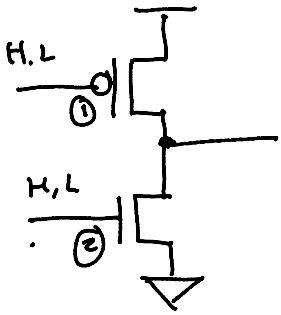
$$\frac{P_1}{P_{50}} = \frac{c \cdot 1 \cdot v^2}{c \cdot 50 \cdot v^2} = 2\%$$

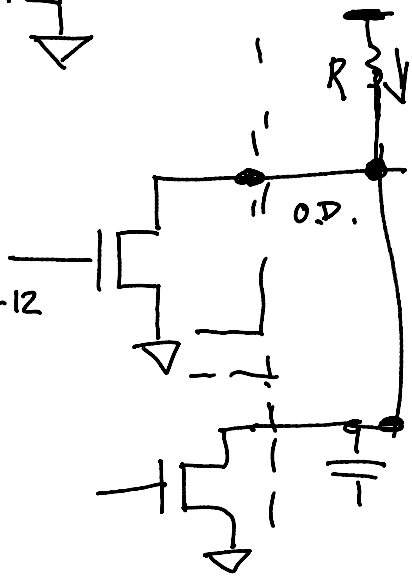
e.g. battery powered watch 32,768 Hz

Exercise 6: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?



①	H	L	H
②	H	L	L
o/p	L	H	Z





$R = 10k$

$C = 50pF$

$V_{dd} = 3.3V$

$RC = 10 \times 10^{3} \cdot 50 \times 10^{-12}$

$= 560 \times 10^{-9}$

$= 0.5 \times 10^{-6}$

$i = \frac{V}{R} = \frac{3.3}{10k} = 0.3mA$?