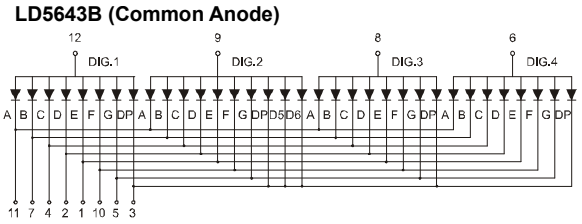
Multiplexed Display

Version 3: Alternate current-limiting resistor configuration and resistors changed to 200 Ω.

Introduction

We can reduce the number of I/O pins required by time-multiplexing them. In this lab you will display the last four digits of your BCIT ID on a 7-segment LED display that has four multiplexed digits.

Your ELEX 2117 parts kit contains an LD5643BR (or compatible) display. It has one anode per digit but the cathodes for each segment are connected together as you can see from the schematic: [1]



To display a number in a particular digit position your circuit must set the corresponding anode to a high voltage and set the cathodes of the segments that are to be lit to a low voltage.

To display more than one digit your circuit must cycle through the four positions, displaying the appropriate digit in each position. If this is done fast enough then all four digits appear to be on continuously.

The frequency at which you cycle through the digits should be high enough that you cannot see the LEDs turn on and off[2]. However, the period should be long enough that the duty cycle is not affected by the rise and fall times of the circuit. 100 Hz is above most people's flicker fusion threshold.

Components

You will need:

- your EPM240T100C5 CPLD board, Byte Blaster JTAG interface and coaxial power connector,
- a solderless breadboard
- four 200 Ω resistors (in your ELEX 2117 parts kit)
- 12 pin-header jumpers (8 for the segment cathodes and four for the digit anodes)
- an LD5643BR 4-digit 7-segment common-anode LED display (or equivalent)

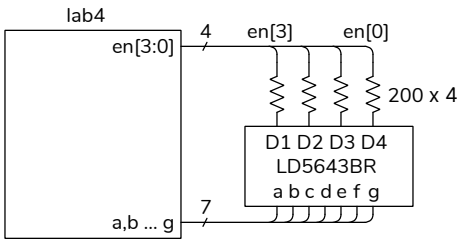
Requirements

Your circuit should show the last four digits of your BCIT ID on the display.

Each digit should be displayed at a frequency of $100+n$ Hz where n is the last two digits of your BCIT ID number. Since there are four digits, your circuit must divide the 50 MHz clock by $\frac{50\times10^6}{4\cdot(100+n)}$.

CPLD I/O

The following diagram shows the connections to the CPLD:

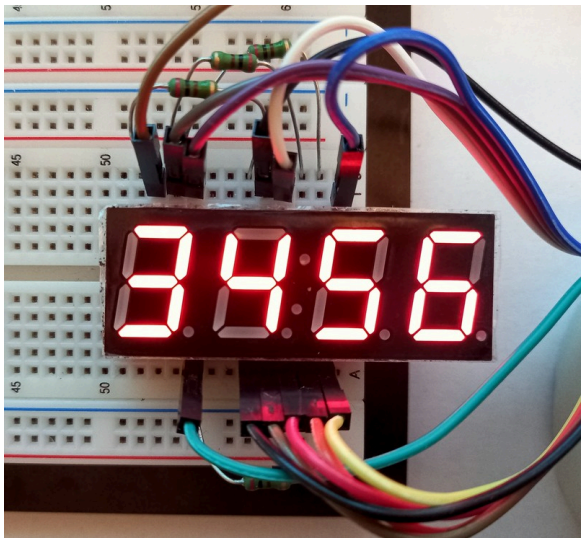


You may use any pin assignments. You can use the one shown below if you want to save time. The sequence of wire colour codes follows the LED pin numbers.

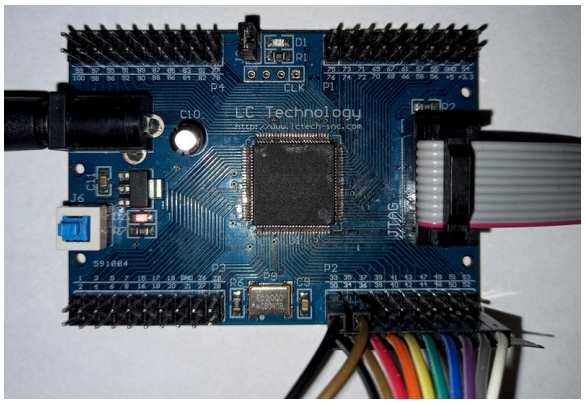
[1] Diagram from LD5463 datasheet.
[2] This is called "flicker."

LED Pin	wire color	segment	CPLD pin
1	black	`e`	30
2	brown	`d`	34
3	red	`dp`	36
4	orange	`c`	38
5	yellow	`g`	40
6	green	`en[0]`	42
7	blue	`b`	44
8	violet	`en[1]`	48
9	gray	`en[2]`	50
10	white	`f`	52
11	black	`a`	33
12	brown	`en[3]`	35

The wiring to the 7-segment LED is shown below:



and the connections to the CPLD pin headers is:



Note that this display has 12 pins. The decimal points (DP) are not connected and pin 3 instead controls the colon. You can force this signal high (1).

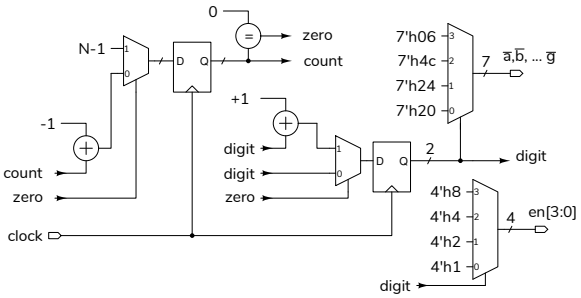
As explained in an earlier lab, using a single current-limiting resistor on the anode causes the LED brightness to vary with the number of segments that are lit and is not the correct way to drive an LED display. Since the forward voltage drop across the LEDs is about 2 V, the voltage across the 200 ohm resistors is about 1.3 volts and the peak current is about $1.3/200 \approx= 6$ mA. Since this is divided across four digits, the average current per digit is about 1.5 mA.

See the alternate in Appendix A if you would like a brighter display at the expense of having to use an additional 3 resistors.

The display datasheet[3] states the maximum current per segment is 25 mA. The 1.5 mA we are supplying is divided among the segments and so the display is operating at a small fraction of it's rated current.

Sample Design

A design that meets the requirements is given below:



The clock divider is similar to that in the previous lab: `count` is a counter that counts down. `zero` is asserted when `count` is zero. The next counter value ("`count_next`") is set to `N-1` when the count reaches `zero`. Thus the `count` register is always counting down from `N-1` to zero and the `zero` output is enabled once every `N` clock cycles – at a rate of 50 MHz divided by N.

`digit` is a 2-bit counter that counts up each time `zero` is asserted. One multiplexer enables the digit-enable output corresponding to the value of `digit`. Another multiplexer selects one of four 7-bit active-low values to turn on the appropriate segments for the `digit`'th number to be displayed.

[3] Available on the course website.

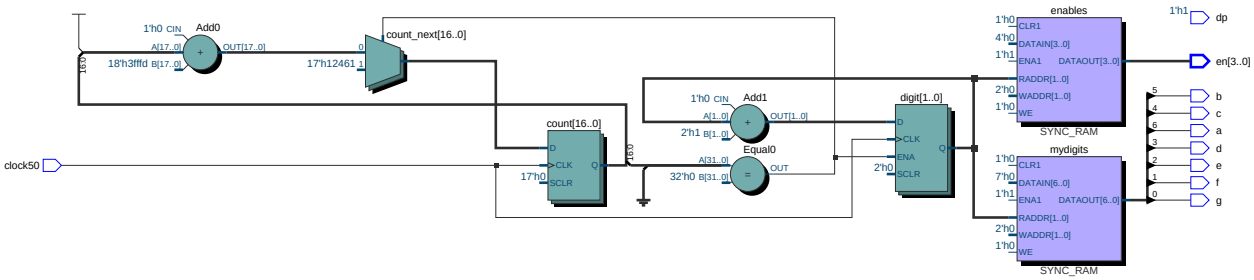


Figure 1: Example RTL Schematic for Lab 4.

Procedure

Write a Verilog module corresponding to the block diagram above or another one that meets the requirements above.

Follow the procedure in Appendix A of lab 1 to create a project, compile it, and configure your CPLD. Assign pin 12 to the 50 MHz oscillator input (`clock` above).

If you follow the wiring shown in the table above you would have the following pin assignments, possibly using different signal names:

To	Assignment Name	Value
a	Location	PIN_33
b	Location	PIN_44
c	Location	PIN_38
clock50	Location	PIN_12
d	Location	PIN_34
dp	Location	PIN_36
e	Location	PIN_30
en[3]	Location	PIN_35
en[2]	Location	PIN_50
en[1]	Location	PIN_48
en[0]	Location	PIN_42
f	Location	PIN_52
g	Location	PIN_40

Test your design.

Submission

To get credit for completing this lab, submit the following to the Assignment folder for Lab 4 on the course website:

1. A PDF document containing:
   - Your name, BCIT ID, course number and lab number.
   - Show how you calculated the clock divider value. Note that this will be different for each student.
   - A listing of your Verilog code. You must follow the coding guidelines given on the "Course Information" section of the course website. Note that these may have changed.

     The listing should be included as text rather than images.
   - a screen capture of your compilation report (**Window > Compilation Report**) similar to this:

     Flow Summary

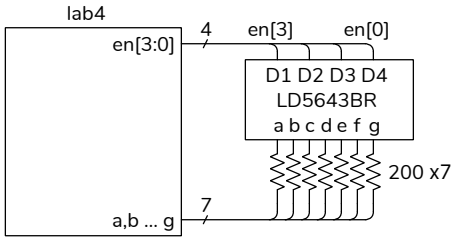
     <<Filter>>

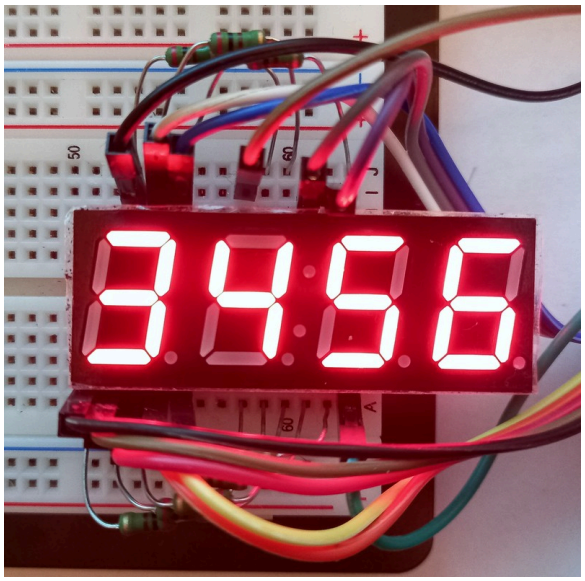
Flow Status	Successful - Wed Oct 07 19:20:41 2020
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	lab4
Top-level Entity Name	lab4
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	42 / 240 (18 %)
Total pins	13 / 80 (16 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

   - a photo of your breadboard distinctly showing the last four digits of your BCIT ID on the four LEDs. Since the LEDs are relatively dim, you may need to dim the room lights to get a good image.
2. The PDF file containing the schematic created by **Tools > Netlist Viewers > RTL Viewer** and then **File > Export...** . The file might look like Figure 1.

A Per-Segment Current Limiting Resistors

Using a current-limiting resistor per segment results in a current (and brightness) that does not vary with the number of segments lit. The disadvantage is needing one resistor per segment (7) instead of one per digit (4). A schematic and a photo of this optional configuration are shown below.





In this case the peak current per segment is about 3 mA. Not using current limiting resistors results in a peak current of about 25 mA which exceeds CPLD and LED absolute maximum ratings. This should be avoided.