ELEX 2117 : Digital Techniques 2
2020 Fall Term

Timers and Clock Dividers

Introduction

Circuits that measure time by counting clock cycles are called timers. Circuits that generate periodic outputs using timers are called clock (or frequency) dividers.

In this lab you will use a frequency divider to generate tones by periodically switching the current flowing through a speaker.

The time between switching the speaker current on and off will be determined by counting cycles of the f_{clock} = 50 MHz clock on the CPLD board. The number of clock cycles required for a period T is T/f_{clock}. The time between switching the speaker between on and off is half of that. For example, for tone frequency of 1 kHz, the waveform period is $\approx f_{clock} = 50{\times}10^6/1000$ =50,000 clock cycles and the time between switching the speaker output should correspond to 25,000 clock cycles.

Components

You will need:

- a solderless breadboard
- your EPM240T100C5 CPLD board, Byte Blaster JTAG interface and coaxial power connector,
- a 1 kΩ resistor
- two SPDT pushbutton switches and machine-pin DIP socket for mounting the switches (two SPST N.C. switches will also work)
- 5 pin-header jumpers
- a speaker[1]
- two cables with alligator clips from your ELEX 1117 parts kit

[1] If you don't have the one from the ELEX 2117 parts kit yet, headphones will probably work.

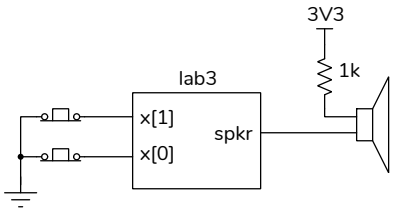
Specifications

Pushing either button should result in a tone being generated. The tone's frequency is determined by the button and the last digit of your BCIT ID:

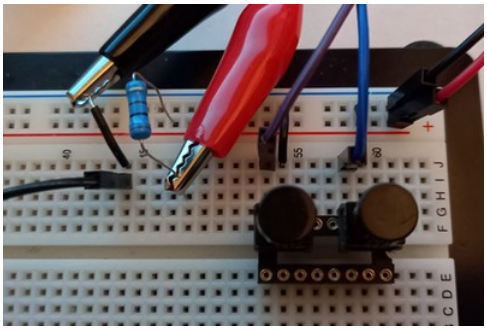
	Frequency for:	
last digit of ID	Left Button	Right Button
0,1,2	220	880
3,4	440	1760
5,6,7	1760	440
8,9	880	220

CPLD I/O

The following diagram shows the connections to the CPLD:



Wire two pushbutton switches and a current-limiting resistor on the breadboard:

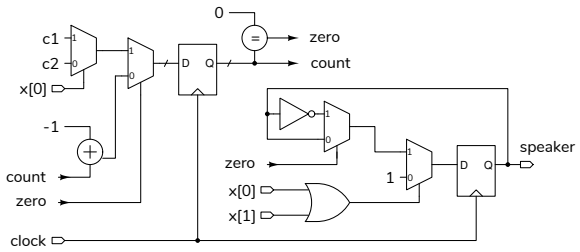


and connect a CPLD I/O pin and the resistor to the speaker with alligator clip cables:

The pin assignments are similar to the previous lab. The switch inputs are configured with pull-ups. The switches are wired so the pushbuttons are active-high (use the normally-closed contacts).

The current-limiting resistor avoids exceeding the maximum current rating of the MAX II CPLD outputs (25 mA)[2]

Sample Design



`count` is a counter that counts down. `zero` is asserted when `count` is zero. The next counter value ("`count_next`") is set to `count`−1, `c1` or `c2` depending on the value of `x[0]` and `zero`. Thus the `count` register is always counting down from either `c1` or `c2` to zero.

`speaker` is toggled (changed to the opposite value) when `zero` and either `x[0]` or `x[1]` are asserted. This results in a waveform with a period of 2`c1` or 2`c2` times the period `clock` (20 ns).

`c1` and `c2` must be calculated to meet the specifications above and `count` must be declared to have enough bits to store the largest of `c2` and `c1`.

Procedure

Write a Verilog module corresponding to the block diagram above or another one that meets the requirements.

[2]See page 5-1 of the MAX II datasheet available on the course web site.

Follow the procedure in Appendix A of lab 1 to create a project, compile it, and configure your CPLD. Assign pin 12 to the 50 MHz oscillator input (`clock` above).

If you use the same switch pins as in the previous lab and Pin 30 for the speaker output, you should end up with the following assignments, possibly using different signal names:

To	Assignment Name	Value	
clk50	Location	PIN_12	Y
spkr	Location	PIN_30	Y
x[1]	Location	PIN_99	Y
x[0]	Location	PIN_97	Y
x[0]	Weak Pull-Up Resistor	On	Y
x[1]	Weak Pull-Up Resistor	On	Y

Test your design.

Submission

To get credit for completing this lab, submit the following to the Assignment folder for Lab 3 on the course website:

1. A PDF document containing:
   - Your name, BCIT ID, course number and lab number.
   - A listing of your Verilog code. You must follow the coding guidelines given on the "Course Information" section of the course website. Note that these may have changed.

     The listing should be included as text rather than images.
   - a screen capture of your compilation report (**Window** > **Compilation Report**) similar to this:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Fri Oct 02 18:38:16 2020
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	37 / 240 (15 %)
Total pins	4 / 80 (5 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

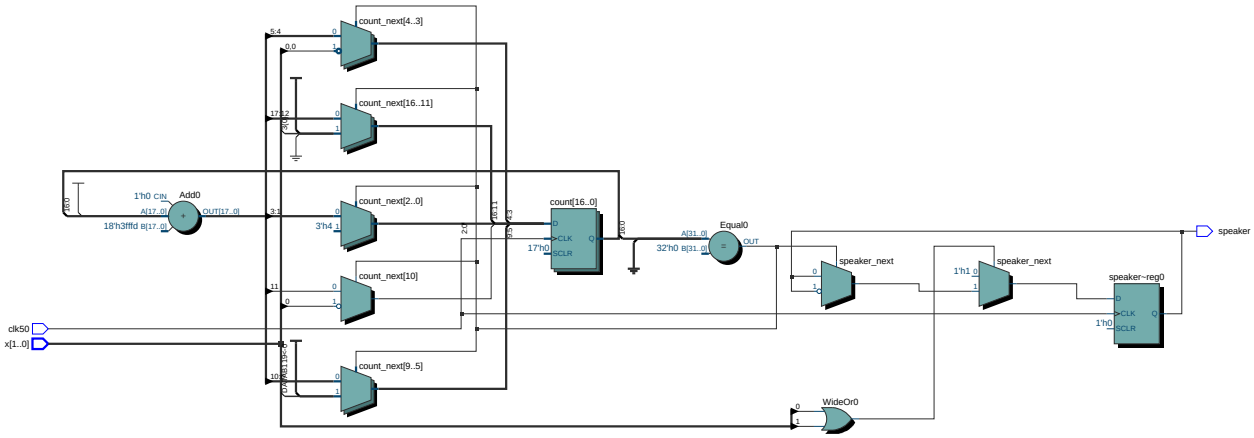


Figure 1: Example RTL Schematic for Lab 3.

2. The PDF file containing the schematic created by **Tools > Netlist Viewers > RTL Viewer** and then **File > Export...** . The file might look like Figure 1.

3. A short video with audio of the tones generated when each of the two pushbuttons are pushed.