Dec. 4 Review Lecture

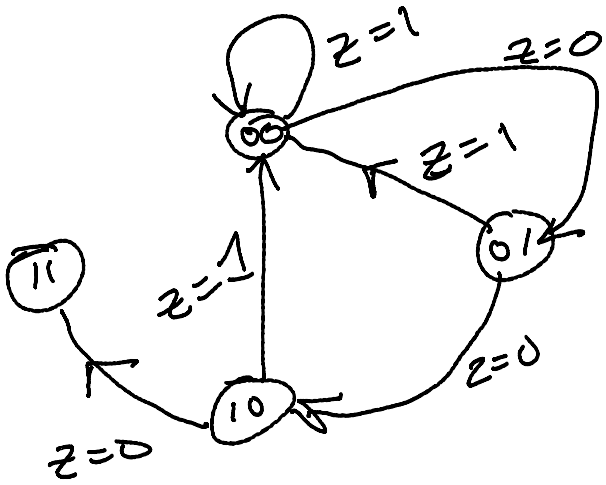
```
module q2 (input logic z, clk) ;

   logic [1:0] x, x_next ;

   always_comb begin
      if ( z && x != 2'b11 )
        x_next = 2'b00 ;
      else if ( x == 2'b00 )
        x_next = 2'b01 ;
      else if ( x == 2'b01 )
        x_next = 2'b10 ;
      else if ( x == 2'b10 )
        x_next = 2'b11 ;
      else
        x_next = x ;
   end

   always_ff @(posedge clk)
     x = x_next ;

endmodule
```



The state transition table below corresponds to the System Verilog state machine description above.

x	z	x_next
00	0	01 ✓
00	1	A 00
01	0	B 10
01	1	00 ✓
10	0	C 11
10	1	00 ✓
11	x	D 11

logic [3:0] [7:0] x;

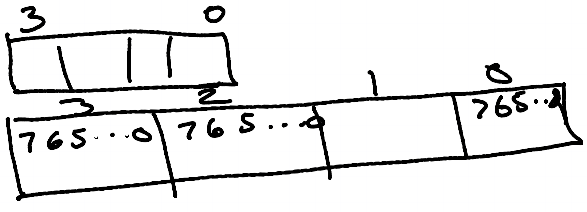
4 words, 8 bits each

logic [3:0] [7:0] x [0:255]

256 words

x [160] [2] [0]

word in memory, byte, bit



= blocking

<= non-blocking

```
always_comb begin
   a=1 ;
   b=2 ;
   c=3 ;
   c <= a ;
   a <= b ;
   b <= c ;
end
```

a	b	c
X	Z	B
→ 1		
→ 2	→ 3	
2	3	1

logic [3:0] y [4]; [0:3]

4'h6 = 4'b0110

assign y = { 4'h3, 4'h9, 4'h6, 4'hc } ;

assign x = y[2][1:0] ;

Give your answer as a two-digit decimal value (00 to 99).

x = 2'b10 = 2

Q2

What is the value assigned to x by the following System Verilog expression:

logic [15:0] y ;

assign y = 16'hf0f0 ;

assign x = 4'h6 & 4'b1 ? y[15:12] : y[3:0]

Give your answer as a two-digit decimal value (00 to 99).

&& logical and

use for true, use this for false

4'h6 = 0110

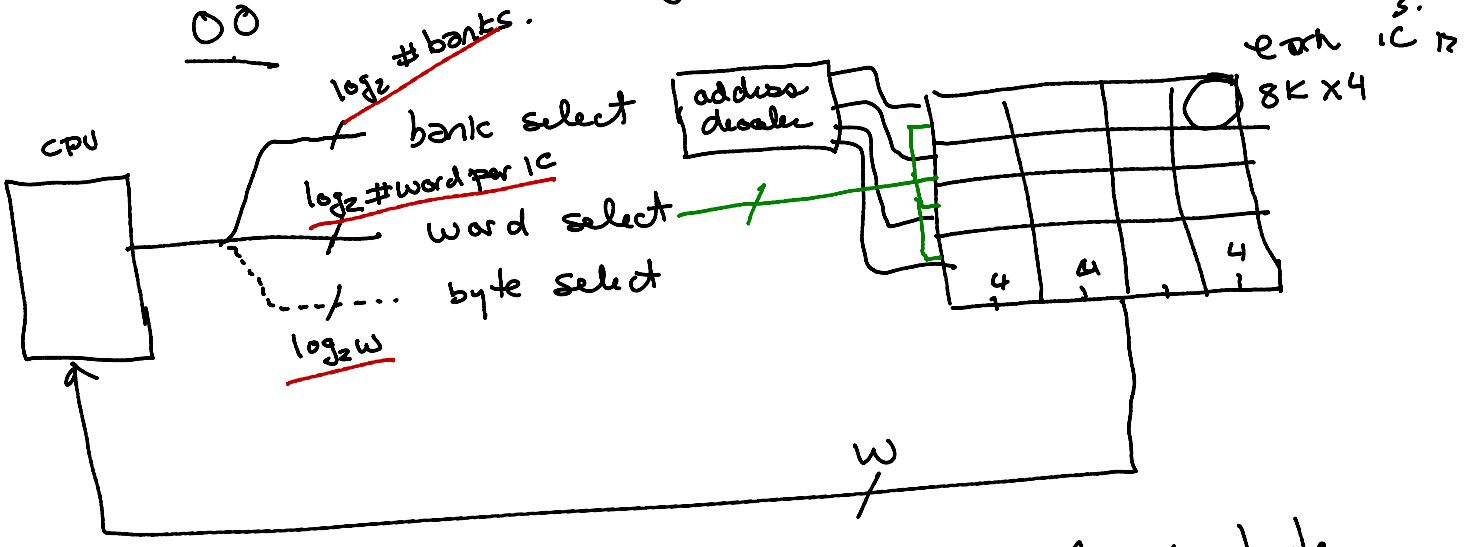
& 4'b1 = 0001

0000

16'hf0f0 = 1111 0000

y[3:0] = 0000

Q0



w = 16

2 bytes / word log2 2 = 1

A0 is byte select

log2 8k = 13 bits for word select

A1 -- A13 for word select

log2 4 = 2 bits for bank select

A14 .. A15