74LS165

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ls165.vxi
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Wilson Li

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8-Bit Parallel-to-Serial Shift Register
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Module 0

Pod 0: A Outside Left
Timing Pod 0/01 [Timing]

Port 0

7:	N/C	Unused Control 7
6:	N/C	Unused Control 6
5:	N/C	Unused Control 5
4:	N/C	Unused Control 4
3:	N/C	Unused Control 3
2:	N/C	Unused Control 2
1:	Output	CP2
0:	Output	CP1
RDY:	N/C	External Signal!
TRG:	N/C	External Signal!

Port 1

9:	N/C	Unused Q 9
8:	N/C	Unused Q 8
7:	N/C	Unused Q 7
6:	N/C	Unused Q 6
5:	N/C	Unused Q 5
4:	N/C	Unused Q 4
3:	N/C	Unused Q 3
2:	N/C	Unused Q 2
1:	N/C	External Signal!
0:	N/C	External Signal!

Module 1

Pod 2: D N/C N/C
Data Pod 2/23 [Pattern I/O]

Port 2

0:	N/C	Unused Pin 17
1:	N/C	Unused Pin 18
2:	N/C	Unused Pin 19
3:	N/C	Unused Pin 20
4:	N/C	Unused Pin 21
5:	N/C	Unused Pin 22
6:	N/C	Unused Pin 23
7:	N/C	Unused Pin 24
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Port 3

0:	N/C	Unused Pin 25
1:	N/C	Unused Pin 26
2:	N/C	Unused Pin 27
3:	N/C	Unused Pin 28
4:	N/C	Unused Pin 29
5:	N/C	Unused Pin 30
6:	N/C	Unused Pin 31
7:	N/C	Unused Pin 32
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Pod 1: D N/C N/C
Data Pod 1/01 [Pattern I/O]

Port 0

0:	N/C	Unused Pin 1
1:	N/C	Unused Pin 2
2:	N/C	Unused Pin 3
3:	N/C	Unused Pin 4
4:	N/C	Unused Pin 5
5:	N/C	Unused Pin 6
6:	N/C	Unused Pin 7
7:	N/C	Unused Pin 8
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Port 1

0:	N/C	Unused Pin 9
1:	N/C	Unused Pin 10
2:	N/C	Unused Pin 11
3:	N/C	Unused Pin 12
4:	N/C	Unused Pin 13
5:	N/C	Unused Pin 14
6:	N/C	Unused Pin 15
7:	N/C	Unused Pin 16
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Module 2

Pod 4: C Outside Right
Data Pod 4/23 [Pattern I/O]

Port 2

0:	Output	PL
1:	Output	DS
2:	N/C	Unused Pin 51
3:	N/C	Unused Pin 52
4:	N/C	Unused Pin 53
5:	N/C	Unused Pin 54
6:	N/C	Unused Pin 55
7:	N/C	Unused Pin 56
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Port 3

0:	N/C	Unused Pin 57
1:	N/C	Unused Pin 58
2:	N/C	Unused Pin 59
3:	N/C	Unused Pin 60
4:	N/C	Unused Pin 61
5:	N/C	Unused Pin 62
6:	N/C	Unused Pin 63
7:	N/C	Unused Pin 64
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Pod 3: C Outside Left
Data Pod 3/01 [Pattern I/O]

Port 0

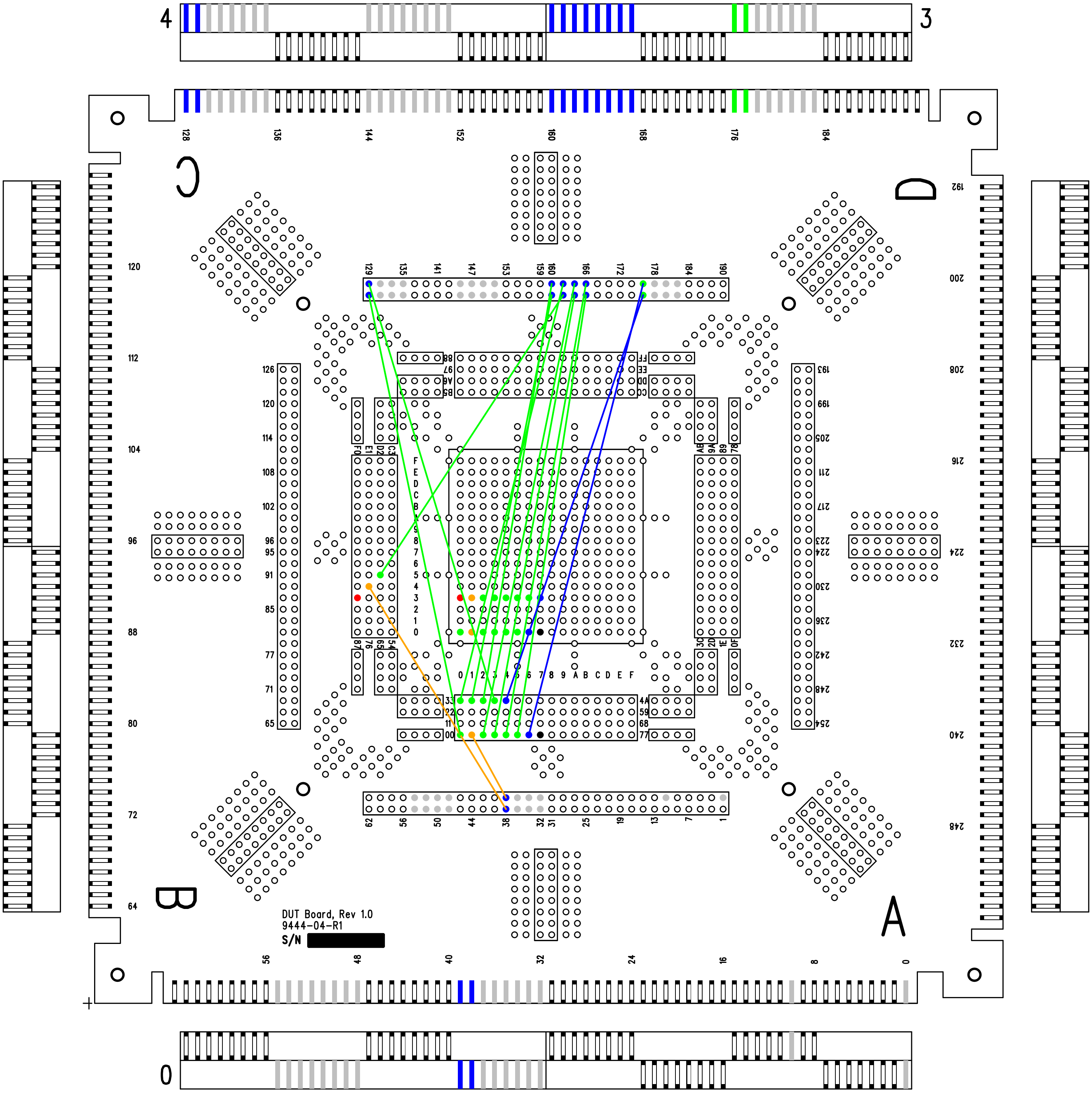
0:	Output	P<0>
1:	Output	P<1>
2:	Output	P<2>
3:	Output	P<3>
4:	Output	P<4>
5:	Output	P<5>
6:	Output	P<6>
7:	Output	P<7>
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

Port 1

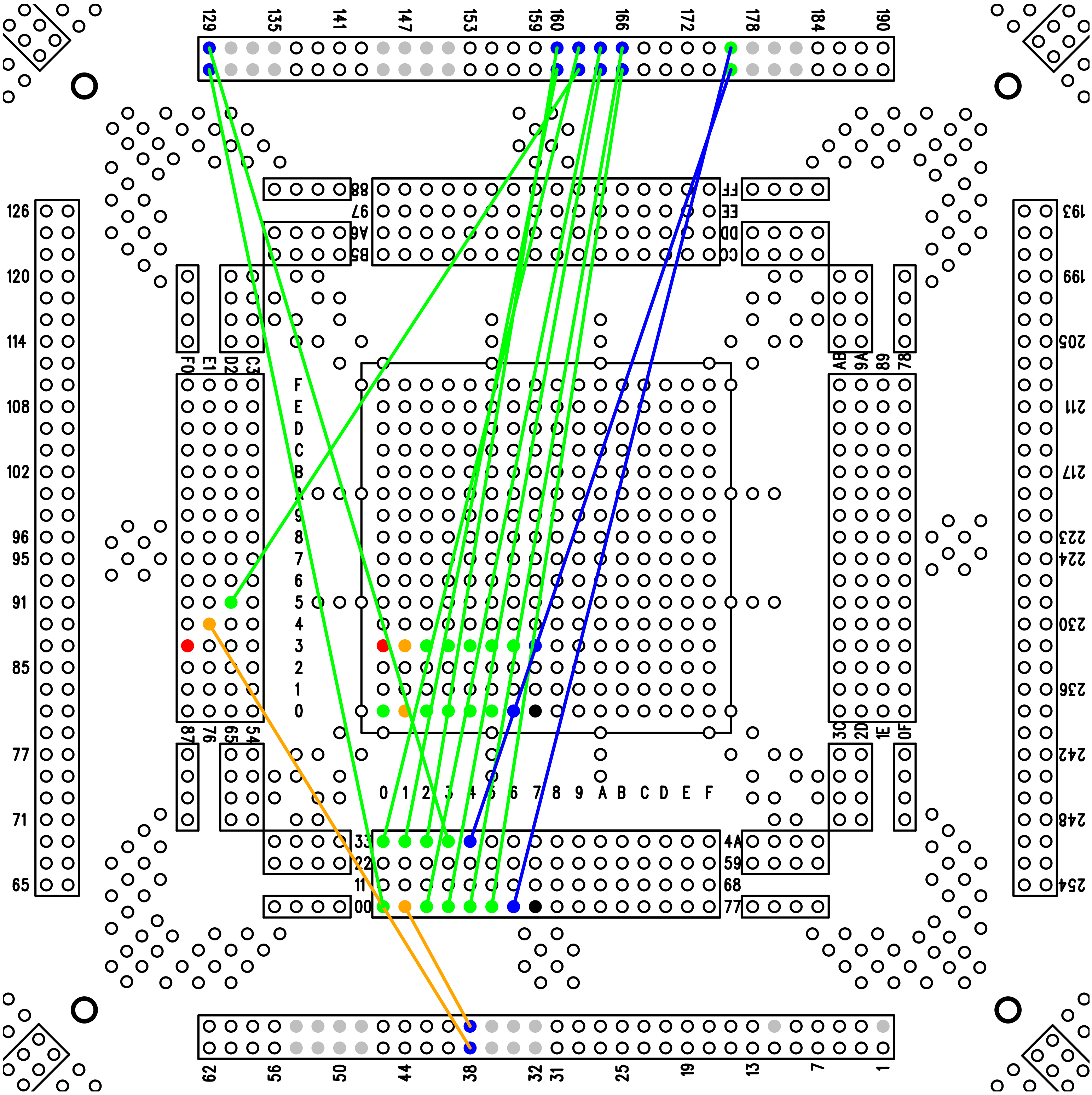
0:	Input	Q<7>_Bar
1:	Input	Q<7>
2:	N/C	Unused Pin 43
3:	N/C	Unused Pin 44
4:	N/C	Unused Pin 45
5:	N/C	Unused Pin 46
6:	N/C	Unused Pin 47
7:	N/C	Unused Pin 48
~OE:	N/C	External Signal!
CLK:	N/C	External Signal!

IC	Signal Name	IWA	OWA	POD_##	
1	PL	00	128	2:0	4
2	CP1	01	39	0:0	0
3	P<4>	02	164	0:4	3
4	P<5>	03	165	0:5	3
5	P<6>	04	166	0:6	3
6	P<7>	05	167	0:7	3
7	Q<7>_Bar	06	176	1:0	3
8	GND	07			
9	Q<7>	37	177	1:1	3
10	DS	36	129	2:1	4
11	P<0>	35	160	0:0	3
12	P<1>	34	161	0:1	3
13	P<2>	33	162	0:2	3
14	P<3>	32	163	0:3	3
15	CP2	31	38	0:1	0
16	VCC	30			
IC	Signal Name	IWA	OWA	POD_##	

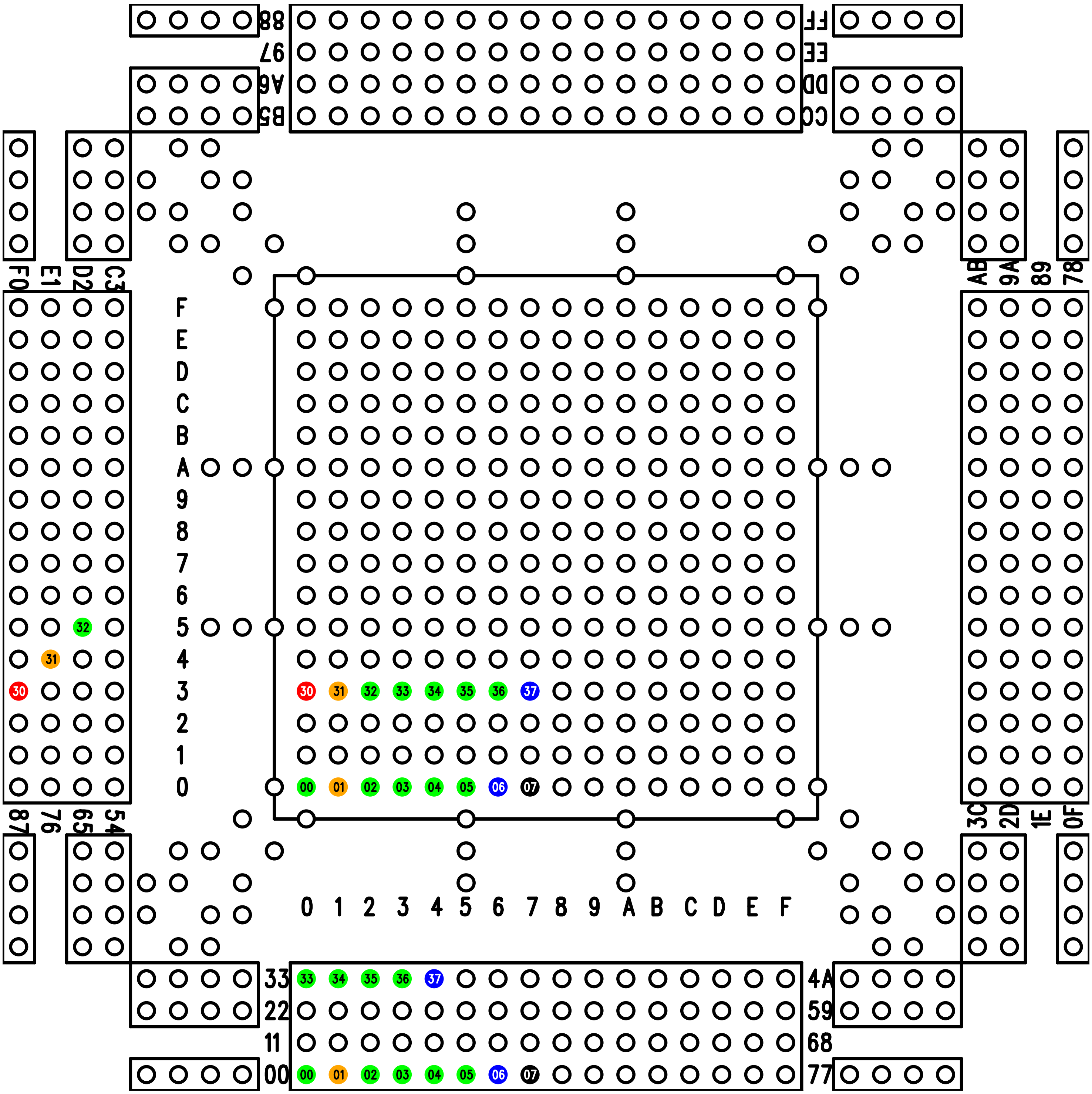
Connector - Pod View



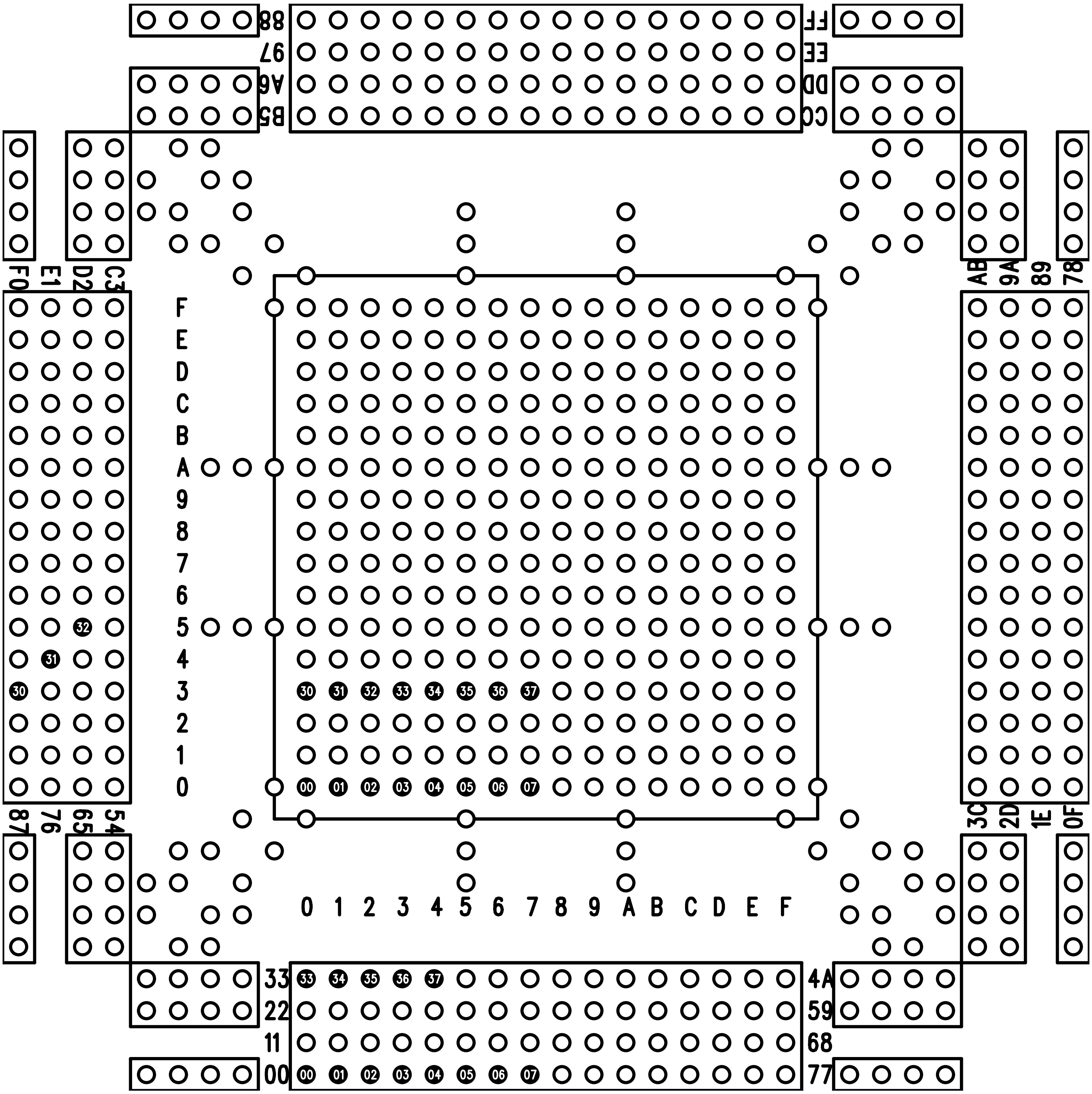
Inner Wiring Array - Outer Wiring Array View



Inner Wiring Array Reference View (Colour)



Inner Wiring Array Reference View (B&W)



IC - PGA Socket View