A Compact Dual-Core 26.1-to-29.9GHz Coupled-CMOS LC-VCO with Implicit Common-Mode Resonance and FoM of –191 dBc/Hz at 10MHz

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***Abstract* — A compact dual-core, single-transformer, and low-power voltage-controlled oscillator (VCO) is presented. The single transformer provides resonance at both differential and common modes, eliminating the need for an explicit inductor for the common-mode resonance. It is implemented vertically using two top metal layers, resulting in significant area saving compared to the state-of-the-art. The LC-tank has common mode resonance at twice the VCO frequency, hence reducing the flicker noise corner frequency of the VCO to 450 kHz. A fully-balanced complementary coupled-Class-C design improves efficiency, maintains symmetric swings across the transformer, and improves reliability. A prototype 26.1-to-29.9 GHz VCO, suitable for 5G applications, is implemented in a 65-nm CMOS process occupying an area of 0.04 mm^2. The VCO consumes 3.4 mW at 27.45 GHz and exhibits a phase noise of –127.5 dBc/Hz at 10 MHz offset resulting in an FoM of −191 dB/Hz.**

***Index Terms* — Voltage-controlled oscillator, low phase noise, , 5G, Coupled-Class-C, common-mode resonance**

I. Introduction

The mm-wave frequency band has recently gained tremendous popularity for wireless communications. The availability of wide bandwidth has made this band attractive for high-data-rate wireless applications such as the 5G new radio (NR). Low power, low phase noise (PN) oscillators are pivotal for the implementation of such systems in a low-cost CMOS process. As the industry moves towards advanced CMOS nodes, the shrinking power supply voltage and increasing flicker noise corner pose significant challenges to the design of low-PN CMOS *LC*-VCOs with a limited power budget [1]–[11].

For any given VCO architecture, the figure of merit (FoM) is proportional to the tank quality factor (Q) and the product of the voltage and current efficiencies ($\eta_v \times \eta_I$) [4]–[6]. Utilizing the common-mode (CM) resonance of a second LC tank which is tuned at $2f_{osc}$, is a well-known technique to improve the PN performance of the LC-VCOs and a powerful tool to approach the maximum thermodynamically achievable FoM [1], [4]. However, this approach has two main drawbacks. First, the design needs two inductors, one tuned at f_{osc} and the other at CM frequency, $f_{r\text{-}CM} = 2.f_{osc}$, resulting in a large footprint [1], [5]. Second, the CM frequency deviates from the tank resonance frequency over the tuning range, diminishing the effectiveness of this approach.

To benefit from the CM resonance technique in nullifying the flicker noise while using only one inductor, one can use the implicit-common-mode (ICM) resonance technique [7] where the

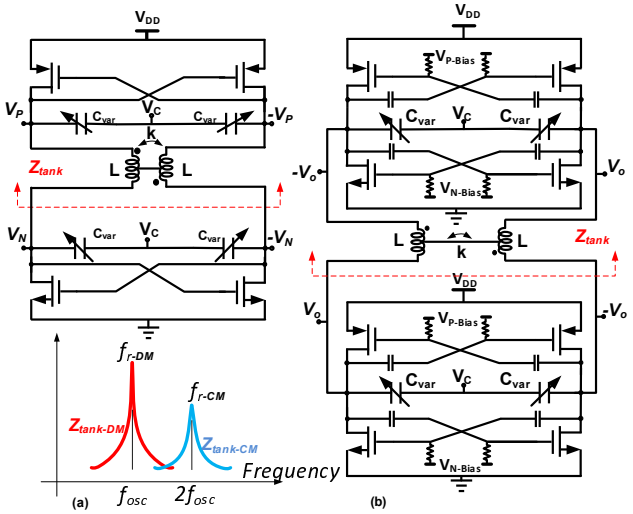

Fig.1. Simplified view of (a) conventional complementary [7] and (b) the proposed coupled-class-C balanced-complementary ICM VCO

equivalent LC-tank of the entire circuit has $f_{r\text{-}CM}$ equal to $2f_{osc}$ and achieves the same flicker-cancellation effect as in [1] (Fig. 1(a)). This approach splits the complementary G_m cores across the LC tank; and hence the signal swings across the tank can be asymmetric due to the separation of NMOS/PMOS devices. Moreover, the signal swing across the NMOS (or PMOS) pair can exceed the supply voltage by $V_{th}/2$ [7], thus creating electrical over-stress (EOS) and potential long-term reliability issues. To address this issue, placing the LC tank in parallel with the VCO cores obviates the need for an additional flicker-cancellation LC tank while creating a fully-balanced complementary structure with increased symmetry around the LC tank. Furthermore, the oscillation signal swing does not exceed V_{DD}, thereby the reliability concerns are avoided and the use of thick oxide devices will not be necessary. An elegant implementation of fully-balanced complementary design is presented in [8]. The design utilizes quad-core complementary G_m cells and $4.f_{osc}$ common-mode resonance cancellation technique to achieve excellent PN performance but it burns significant amount of power and occupies a large area since it uses four cores that are coupled with a large 4-port transformer. While it is possible to lower the power with fewer cores at the expense of phase noise, the area is not significantly reduced due to the circular design of the transformer. To solve this problem with minimal impact on the phase noise, we propose a fully complimentary dual-core coupled-class-C design

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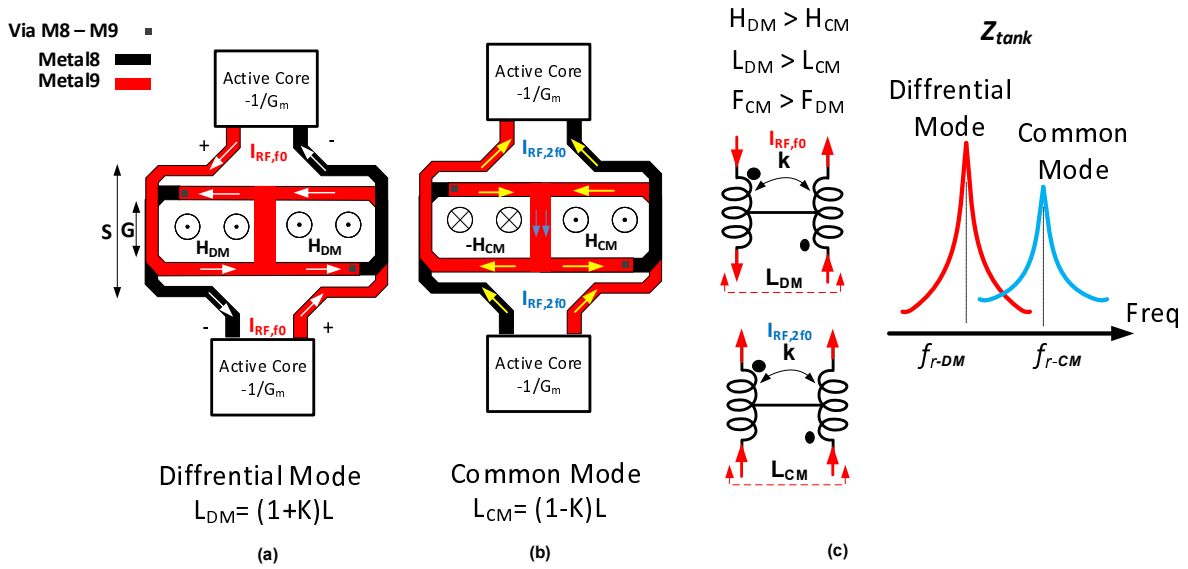


Fig. 2. Proposed 1-turn XFMR and resulting (a) differential- and (b) common-mode currents; (c) simplified lump model of the XFMR

(Fig. 1(b)) with a compact transformer which results in significant power and area savings without sacrificing the close-to-carrier phase noise performance. The remainder of this paper is organized as follows: Section II describes the proposed structure. Section III describes the overall class-C design and the technique to independently adjust the resonant frequency of differential mode (DM) $f_{r\text{-}DM}$ from $f_{r\text{-}CM}$. Section IV presents the measurement results. Section V provides concluding remarks.

II. Proposed Single-Tank ICM VCO Architecture

A simplified topology for the proposed oscillator is shown in Fig. 1(b). The tank is comprised of a single-turn transformer (XFMR) with an impedance of Z_{tank}. The oscillation frequency at the DM resonance of the LC tank is 28 GHz, $f_{r\text{-}DM} = f_{osc} \approx 28$ GHz. The CM impedance ($Z_{tank\text{-}CM}$) has a resonance frequency of twice the oscillation frequency, $f_{r\text{-}CM} \approx 2f_{osc} \approx 56$ GHz, which results in mitigating the flicker noise. As will be shown, $f_{r\text{-}CM}$ alignment with $2f_{osc}$ is done by adjusting the CM and DM capacitances, C_{CM} and C_{DM}, respectively. The active core uses two complementary AC-biased push-pull class-C G_m cells. The bias voltage controls current conduction angle of each branch and keeps the devices in saturation, resulting in an improved current efficiency and performance [5,6].

Fig. 2 shows the operation of the proposed topology using a 1-turn XFMR. The XFMR uses the top two thick metal layers of the 65nm process (M9 and M8). In DM, the current directions on the left and right sides of the XFMR lead to constructive coupling between their corresponding magnetic fields (Fig. 2(a)). However, in CM, as shown in Fig.2(b), the direction of the currents is reversed. As a result, the magnetic fields create a destructive coupling. The resulting difference in magnetic flux between the CM and DM can be modeled by different inductances, namely L_{CM} and L_{DM}, and can be written as:

$$L_{CM} = (1-K)L \quad , \quad L_{DM} = (1+K)L \qquad (1),$$

where K is the coupling factor of the XFMR and can be controlled by layout parameters (dimensions G and S in Fig. 2(a)). Given that the DM and CM resonance frequencies are inversely proportional to their corresponding inductances, and the fact that $L_{CM} < L_{DM}$

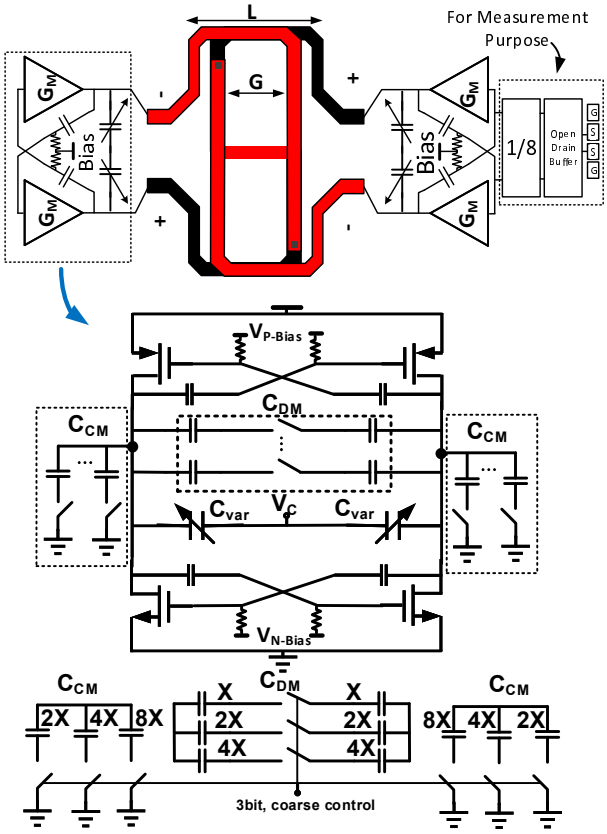
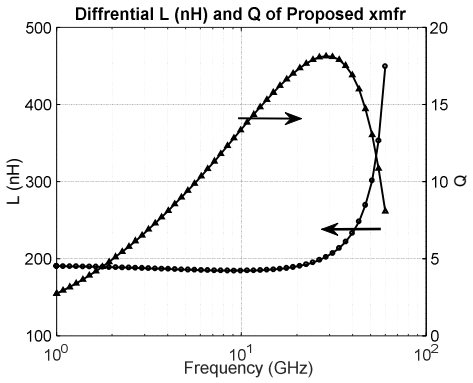
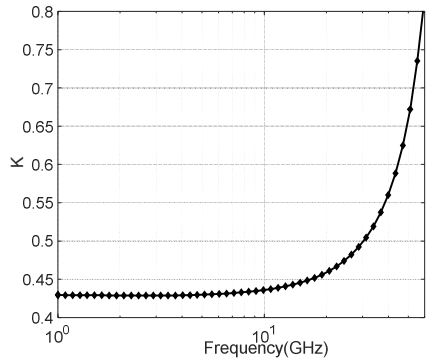


Fig. 3. Proposed dual-core complementary Class-C VCO



(a)



(b)

Fig. 4. Simulated (a) inductance, Q, and (b) coupling factor of the proposed single-turn XFMR

based on (1), this topology can be used to create a higher CM resonance frequency than f_{osc}. Therefore, by careful selection of the tank capacitance and K, $f_{r\text{-}CM}$ can be set to twice the oscillation frequency, that is, $f_{r\text{-}CM}(K, C_{CM}, L_{CM}) = 2f_{osc}$.

The XFMR is optimized to exhibit the highest Q for L_{DM} in the band of interest resulting in simulated $L_{DM} \approx 190$pH (Fig. 4 (a)) with $K \approx 0.45$ between 26 GHz and 30 GHz (Fig. 4 (b)).

III. Adjusting Common-Mode Resonance Frequency

The proposed complimentary ICM resonance VCO with class-C active core is shown in Fig. 3. The active core employs a push-pull complementary structure with independent bias for NMOS and PMOS pairs [5, 6]. By adjusting $V_{N\text{-}Bias}$ and $V_{P\text{-}Bias}$, the conduction angle of the tank current can be shaped to class-C waveform, resulting in improved current efficiency [5–6].

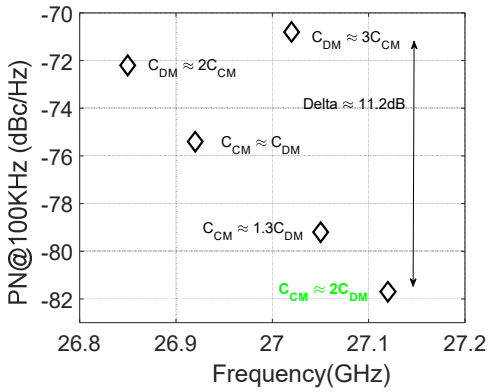


Fig. 5. Simulation results for PN@100KHz for different combination of C_{CM} and C_{DM}

As shown in Fig. 3, two independent 3-bit binary-weighted capacitor banks, namely C_{CM} and C_{DM}, are implemented to adjust fundamental (DM) and CM resonance frequencies. In DM mode, the center point of the circuit is virtual ground and therefore, the overall tank capacitance is $C_{CM} + C_{DM}$. Whereas, in CM mode, the tank capacitance becomes only C_{CM}. By assuming $f_{r\text{-}CM} = 2\, f_{r\text{-}DM}$, the relation between C_{CM} and C_{DM} can be written as:

$$\frac{1}{\sqrt{L_{CM}\, C_{CM}}} = \frac{2}{\sqrt{L_{DM}\,(C_{CM}+C_{DM})}} \Rightarrow \frac{C_{DM}}{C_{CM}} = \frac{3-5K}{1+K} \qquad (2).$$

In the proposed design, the dimensions of XFMR is chosen to provide $K \approx 0.45$, which corresponds to $L_{DM} \approx 184\, pH$ and $L_{CM} \approx 69\, pH$. In this case, (2) can be simplified to $C_{CM} \approx 2C_{DM}$. As shown in Fig. 3, by choosing the unit cells of the binary-weighed C_{CM} bank to be twice as large as C_{DM} bank, one can guarantee that the same code setting for both banks can be used to satisfy $C_{CM} \approx 2\, C_{DM}$ condition. To verify the CM-resonance noise cancelation technique, a PN simulation in the vicinity of 27 GHz and with different combination of C_{CM}/C_{DM} is performed. As shown in Fig.5 the best PN at 100 kHz is achieved when $C_{CM} \approx 2\, C_{DM}$ with ~11.2dB improvement compared to the worst case.

IV. Implementation and Measurement Results

The proposed complimentary ICM-resonance VCO is designed and implemented in a 65nm CMOS process. The die micrograph is shown in Fig. 6. The VCO area (excluding pads) is about 240 × 160 μm^2. The capacitor banks are sized in conjunction with the XFMR so that class-C VCO operates between 26.1-to- 29.9 GHz. The VCO can be coarse programmed by 3 bits, and an accumulation-mode MOS varactor (maximum voltage < 1V) is used for fine tuning with an average K_{VCO} gain of 345 MHz/V over the tuning range. To facilitate the measurements and eliminate RF probes, the output frequency of the VCO is divided by 8, as shown in Fig. 3. The frequency division is done by using three consecutive current-mode-logic (CML) dividers that map the frequency range of 26.1-to-29.9 GHz to 3.26-to-3.73 GHz. The low-frequency outputs are measured using an E5052B Signal

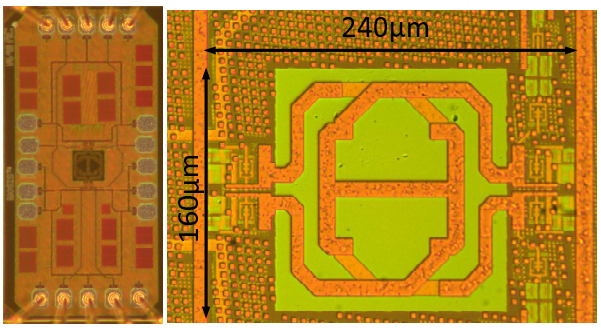


Fig. 6. Die Micrograph of proposed VCO

TABLE I PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-ART

	This Work	ISSCC 2016 [9]	JSSC 2018 [8]	ISSCC 2019 [10]	ISSCC 2019 [10]	JSSC 2018 [11]
CMOS Process / Supply (V)	**65nm / 0.9**	65nm / N/A	40nm / 0.95	65nm / 0.48	65nm / 0.48	28nm / 1
Freq (GHz)	**27.45**	27.5	27	29.92	25.48	28
Tuning Range (%)	**13.4**	18	26	16	16	14
Power (mW)	**3.4**	3.98	16.1	4	3.8	12
PN @100 kHz (dBc/Hz)	**–80.9**	–70	–86*	NA	NA	–83
PN @1 MHz (dBc/Hz)	**–105.7**	–95.3	–109.3	-105.97	-109.24	–106
PN @10 MHz (dBc/Hz)	**–127.5**	–117	N/A	-124.74	-127.9	–126
FoM @100 kHz (dB)	**–184.3**	–173	–182	NA	NA	–181
FoM @10 MHz(dB)	**–191**	−181	−186	–188.2	-190.3	–184
FoM$_T$ @10 MHz (dB)	**–193.4**	−183.4	–194.3	–192.3	-194.4	NA
VCO Area (mm^2)	**0.038**	< 0.1**	0.1	0.08	0.08	0.15

*Estimated based on data at 200 kHz; **Estimated based on the area of the VCO + divider;

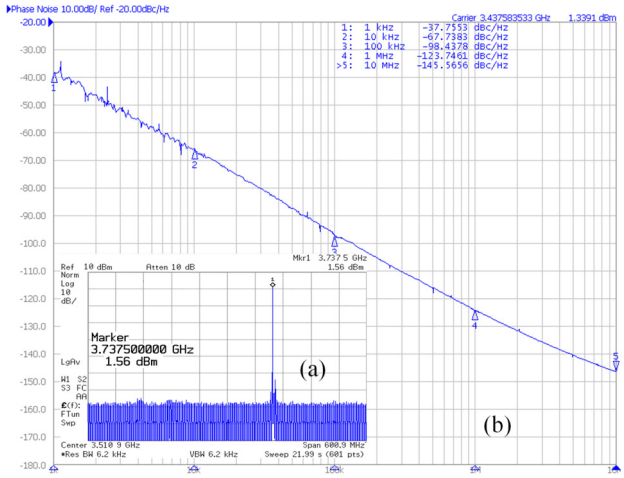


Fig. 7. (a) Measured output spectrum of the VCO operating at 29.9 GHz (highest frequency), (b) Measured PN plot at mid-band (27.45 GHz) with flicker noise corner ≈ 450 kHz

Source Analyzer (SSA). The measured PN at the frequency range of 3.26-to-3.73 GHz is shifted down by 20log(8) ≈ 18.06 dB due to the aforementioned frequency division. As a result, one needs to translate back the measured results by this factor to estimate the VCO's PN in 26.1-to-29.9 GHz range.

Fig. 7 (a) shows the measured output spectrum of the VCO at 29.9 GHz (3.73 GHz at the output of the divider). Fig. 7 (b) shows the measured PN plot at 27.45 GHz with a PN of –105.6 dBc/Hz and −127.4 dBc/Hz at 1 MHz and 10 MHz offset, respectively (after adding 18.06 dBc/Hz to the measured PN values). The flicker-noise corner is interpolated to be around 450 kHz.

Fig. 8 shows the FoM and Frequency Tuning Range (FTR) versus capacitor-bank code. The VCO achieves FTR = 13.4% (varactor voltage is set to $V_{DD}/2 \approx 0.45$ V). The tight variation of FoM over the frequency tuning range suggests that the CM resonance frequency of the tank is properly changed by the capacitor code setting, as discussed in previous section. Table I summarizes the performance of the proposed structure and compares it with the state-of-the-art using the following FoMs:

$$FOM = PN - 20\log(fo/\Delta f) + 10\log(P_{DC}/1mW) \quad (3),$$

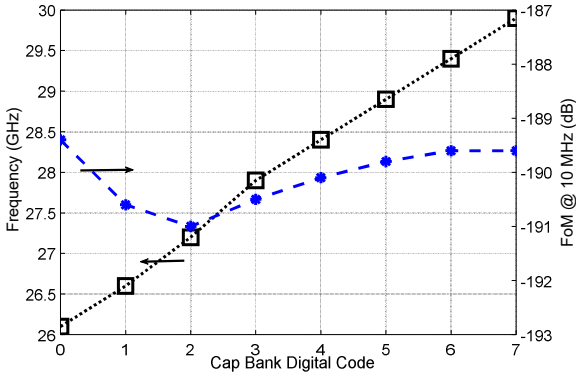


Fig. 8. Tuning range and FoM @ 10 MHz versus capacitor code

$$FOM_T = FOM - 20\log(FTR/10) \quad (4).$$

Based on Table I, the performance of the proposed design compares favorably with that of the state-of-the-art VCOs while achieves smallest are.

IV. CONCLUSION

A compact 28-GHz dual-core coupled-class-C CMOS VCO which employs ICM resonance at the second harmonic of the oscillation using a single XFMR, is presented. Measured results for a 65-nm prototype demonstrate that these techniques result in suppressing flicker-noise, improving efficiency, and maintaining symmetry and reliability. A comparison with the state-of-the-art published designs operating in the same frequency range shows that the proposed design offers superior FoM at 10MHz while occupying less silicon area.

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