A Fully Integrated Multi-Mode High-Efficiency Transmitter for IoT Applications in 40nm CMOS

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***Abstract*—This paper presents a fully integrated multi-mode high efficiency transmitter (TX), employing supply scaling technique using a DC-DC converter to improve the efficiency for low power body area network (BAN) applications while supporting higher power Bluetooth Low Energy® (BLE) applications. The proposed architecture improves the efficiency of the conventional constant-supply switching PAs by a factor of 3 in low power mode, resulting in power saving of nearly 1mW at −10dBm output power. The TX benefits from a compact 0.1mm² PLL operating with an IPN of 0.83° at 2.4GHz and spot phase noise of −119.4dBc/Hz at 3MHz offset. The chip is fabricated in a 40nm LP CMOS process with a die area of 0.7mm². The proposed transmitter consumes 6.1mW at 3dBm output power in BLE mode and 1.6mW at −10dBm for BAN applications, which is, to the best of our knowledge, the lowest reported power consumption among the BLE transmitters in similar process node.**

***Keywords*—Low power wireless, Internet-of-Things (IoT), Bluetooth Low Energy (BLE), Body Area Network (BAN), CMOS, transmitter, switching power amplifier.**

I. Introduction

Internet of Things (IoT) is gaining currency as the next generation technological platform for global connectivity. Ultra-Low-Power (ULP) wireless systems are pivotal in the success of IoT applications. These systems enable both long-range applications such as smart homes and short-range applications such as wireless health monitoring. While Bluetooth Low Energy® (BLE) is the most popular standard for relatively long-range low-power wireless systems [1]-[4], short-range low data-rate medical applications are classified under the Body Area Network (BAN). In order to achieve high-efficiency, most BLE transmitters are optimized for best efficiency at maximum output power above 0dBm which is defined by the standard, inevitably delivering poor efficiency at low output powers (around −10dBm) needed for BAN applications. As IoT sensor nodes are becoming ubiquitous, designing unified systems to support both BLE and BAN with high efficiency is becoming necessary in order to maximize the battery life and avoid the additional cost associated with extra radios. This paper addresses this issue by presenting a multi-mode transmitter system supporting both BLE and BAN.

Switching power amplifier architectures are commonly used for IoT applications since the phase-modulated signals used in such systems do not have any amplitude information. Popular architectures are Class-D [1-4] and Class E/F power amplifiers (PA) [5-6]. Class-D PAs are suitable for applications targeting output powers around 0dBm with robust matching and no reliability concerns. Class E/F PAs usually use cascoding for reliability concerns and more complicated (off-chip) matching network for harmonic suppression [5]. However, the output power control across a wide range (>10dB) remains a challenge.

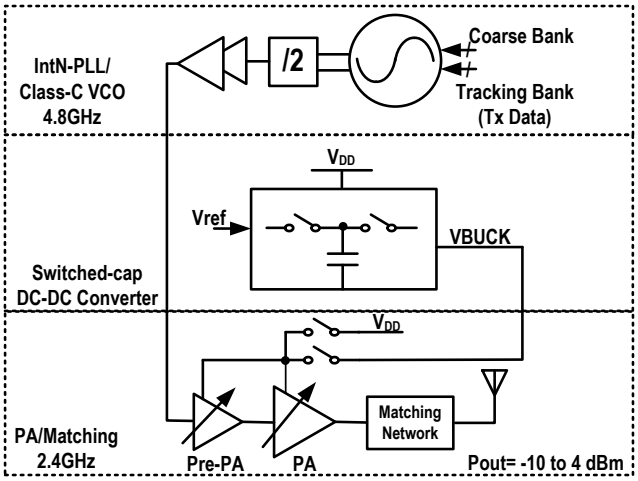

Fig. 1. Block diagram of the proposed low power BLE/BAN transmitter

Varying the supply voltage based on the output power benefits the efficiency of the PA [7]. Manual continuous-time supply variation is not viable for the majority of battery-powered radios [7]. One approach involves using a low drop out (LDO) regulator to vary the supply voltage [5], however, LDO is a linear regulator, which dissipates power across its output transistor and degrades the overall efficiency. Using a switching regulator, on the other hand, helps preserve the efficiency by allowing supply variation with minimal power dissipation. This work presents a fully-integrated low power transmitter in 40nm CMOS which employs load tuning and supply scaling for efficiency improvement in low output power mode. The transmitter system consists of a switched-capacitor DC-DC converter, phase-locked loop (PLL), and power amplifier (Fig. 1). The fully integrated switched-capacitor buck converter is used for supply scaling to improve the efficiency at low power modes intended for BAN applications. The PLL operates at twice the carrier frequency to help eliminate the pulling effect. The remainder of this paper is organized as follows: Section II explains the power amplifier architecture and matching network. Section III elaborates on the design, implementation, and measurement results of the PLL. Section IV discusses the implementation of the DC-DC converter. Transmitter measurement results and conclusions will follow in Section V and Section VI, respectively.

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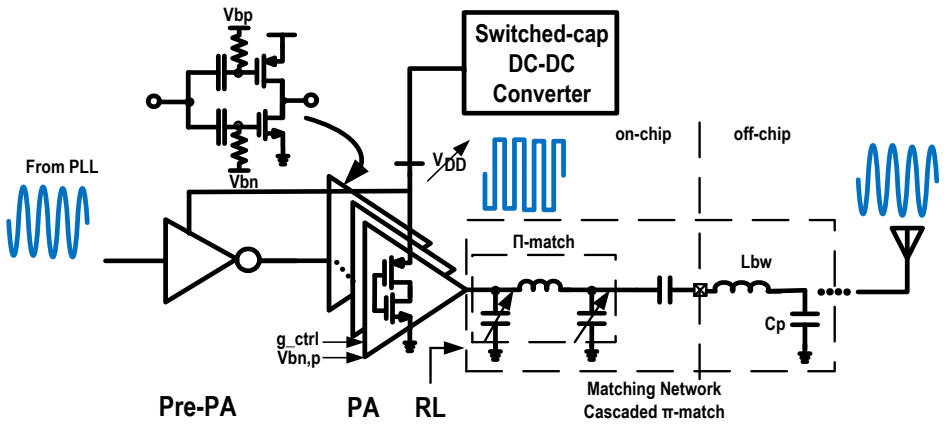

Fig. 2. Block diagram and circuit schematic of the power amplifier, matching network, and bias circuitry.

II. Proposed Power Amplifier/Output Matching

The proposed power amplifier is shown in Fig. 2. Switching PAs are commonly used for constant-envelop signals where Class D or E/F are among the most popular circuit topologies. While parasitic capacitance of switching transistor in class E/F is absorbed in the matching network potentially resulting in higher efficiency, reliability concerns due to high output swings and complicated (off-chip) matching network make them undesirable for low cost fully integrated solutions. A class-D PA does not suffer from above issues. Moreover, in smaller process nodes, transistors become better switches with smaller on-resistance, R_{on}, and negligible parasitic capacitance, making this architecture more suitable for a robust fully integrated solution. The sine wave signal from the VCO becomes a square wave after passing through the inverter chain forming the core of the PA. Upon filtering the signal in the matching network, the sine wave is re-generated. The PA output power and DC power drawn from the supply can be expressed as:

$$P_{out} = \frac{2R_L {V_{DD}}^2}{\pi^2 (R_L + R_{on})^2}, P_{DC} = \frac{2{V_{DD}}^2}{\pi^2 (R_L + R_{on})},$$

where R_L is the loading seen at the output of the PA and R_{on} is the switch resistance, assuming NMOS and PMOS resistances are almost equal. From above equations, the drain efficiency will be:

$$\eta = \frac{R_L}{(R_L + R_{on})},$$

which shows that the loss is dominated by the switch on-resistance whose minimum is set by the maximum output power; also, the efficiency depends on the ratio of the output loading to the switch resistance. There are three ways to decrease the output power:

1) Increase R_{on} by decreasing the number of parallel branches as shown in Fig. 2: this approach increases loss and consequently decreases the efficiency.
2) Increase R_L by tuning the matching network, which transforms the 50-ohm to the desired R_L: among different matching topologies, cascaded π-match offers the best Q and harmonics rejection, and minimum on-chip inductors by utilizing the high-Q bondwire inductance (Q>20) as the second stage of matching network. In our design, a long bondwire with ~3nH inductance was used. Although, tuning R_L by itself should not degrade the efficiency, the loss in tuning capacitors would result in lower measured efficiency.
3) Reducing VDD through a DC-DC converter: this would decrease the output power with negligible impact on the efficiency if the DC-DC converter efficiency is sufficiently high compared to the efficiency of the PA core.

In this work, a combination of all the above three methods are implemented for power control. For high output powers (>0dBm), the DC-DC converter is bypassed as the efficiency degradation due to the loss of the converter outweighs the small improvement in efficiency obtained by supply scaling. The power is varied by adjusting the number of parallel branches. Load tuning is used for fine-tuning. In low power BAN mode (~−10dBm), the DC-DC converter generates half of the nominal supply to improve the efficiency. The transistor gate biases are separated, as shown in Fig. 2, to provide proper operating point for NMOS/PMOS in low VDD regime.

III. Proposed Low Power PLL

Transmitter signal is generated at twice the carrier frequency by an integer-N PLL. As shown in Fig. 3a, the CMOS VCO with programmable PMOS gate-bias is operating at 4.8GHz. $L_{tank} \times Q_{tank}$ is maximized in order to achieve a low power of 150µW. The tuning range of 4.55 GHz to 5.15 GHz is achieved. A quadrature CML divider with resistive load (Fig. 3b) divides the output of the VCO. The design was targeting low phase noise at the offset frequency of 3MHz for the reciprocal mixing of the interferers in the adjacent channel when PLL is shared in the Receive Mode in a BLE transceiver. Placing PLL building blocks inside the VCO inductor reduced its Q slightly by 6% but resulted in total area saving (Fig. 3c). The total power consumption of PLL is 280µW and its Integrated Phase Noise (IPN) from 1kHz to 1MHz is 0.83° (Fig. 3d) with a spot phase noise at 3MHz offset of −119.4 dBc/Hz.

The modulation transmit data is fed into the VCO capacitor bank through its LSB bit, modulating the VCO frequency and generating the phase modulated signal after opening the PLL loop during the Transmit Mode time period.

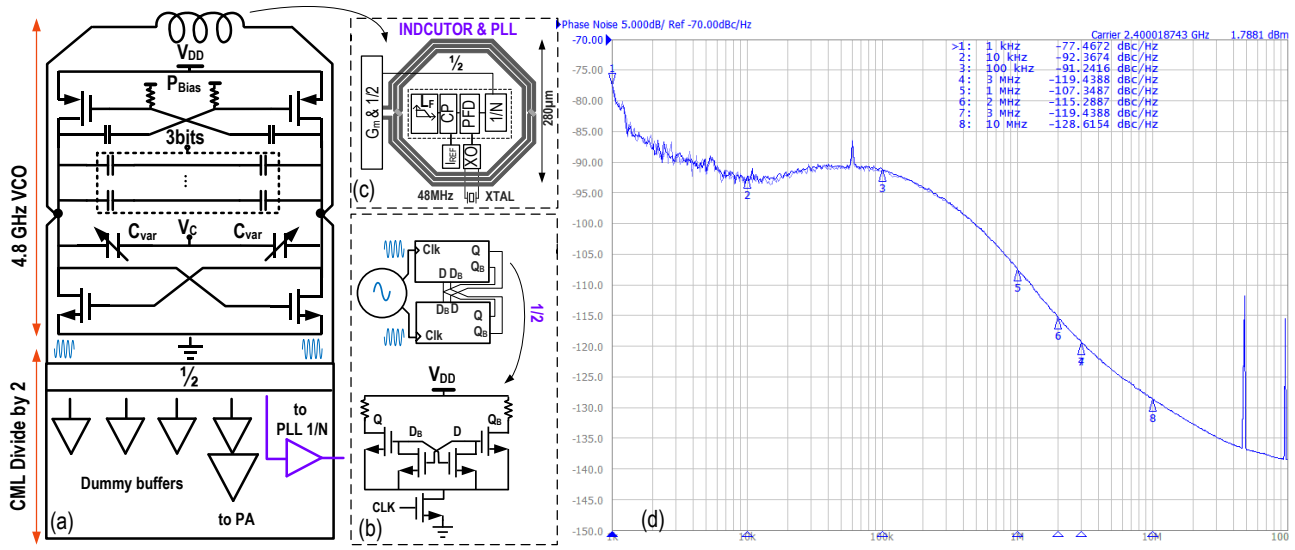

Fig. 3. Proposed phase locked loop (a) VCO, (b) CML divider, (c) block diagram, and (d) measured phase noise of the PLL

IV. SWITCHED-CAPACITOR DC-DC CONVERTER

The integrated switched-capacitor DC-DC converter block diagram is shown in Fig. 4. A fully digital closed-loop architecture is chosen for the buck converter consisting of output switch units, switch drivers, ring oscillator, charge pump, and strong-arm comparator. The sampling clock for the comparator is provided by the oscillator output divided by two obviating the need for an external clock. The fully digital loop is robust and stable. The size of the flying capacitor, C_{fly}, plays an important role in the overall efficiency of the converter. To faciliate integration with miniaturized biomedical implants, die size needs to be very small. As such, a small C_{fly} is chosen resulting in a minor degredation in the efficiency of the converter. All design parameters including the C_{fly}, switching frequency, f_{sw}, switch size and resistance, R_{on}, are optimized for output voltage and loading through initial system level simulations [8].

In order to reduce the ripples at the output of the converter and reducing the in-band spurs at the antenna, multi-phase clocking is used and twelve phases of the ring oscillator's output is fed into the twelve parallel switch unit slices, making the effective switching frequency twelve times higher resulting in significantly smaller ripple on the output voltage.

Another challenge in designing the converter for BLE application is the start-up time. The slow startup time of milliseconds for BLE packets which last only microseconds, results in very poor overall system efficiency. Therefore, a fast charge mode (FC) is added to the charge pump to reduce the startup time below 10µs.

In order to address the ripple vs. settling time trade-off, the charge pump gain is programmable for optimum design point that minimizes the startup time and at the same time, keeps the output spur level below the specification set by the standard.

The design of all circuit blocks in the control loop is optimized for minimum power consumption to achieve the maximum converter efficiency.

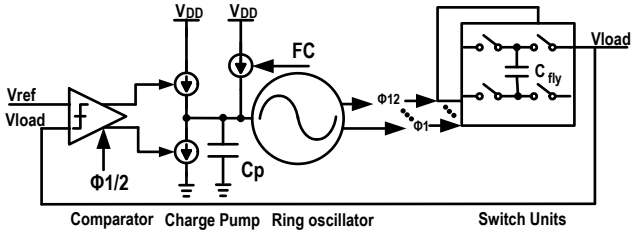

Fig. 4. Switched-capacitor DC-DC converter block diagram

V. IMPLEMENTATION DETAILS AND MEASUREMENT RESULTS

The multi-mode transmitter including the PLL is fabricated in a 40nm LP CMOS process with die area of 0.7mm^2 (Fig. 5). The PCB test board snapshot is also shown in Fig. 5.

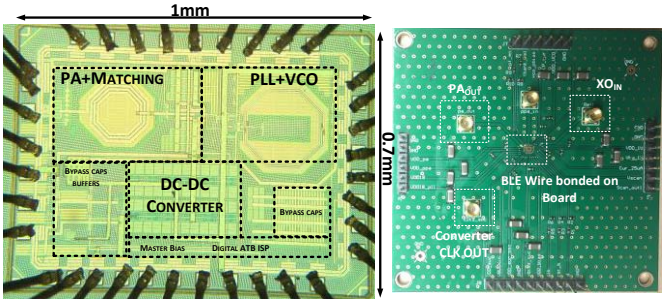

Fig. 5. Die photo and PCB test board of the BLE transmitter.

The DC-DC converter was characterized for different load conditions. The converter reaches the maximum efficiency of 65% at the middle of the output voltage range around half the supply measured at 0.45V, which is very close to simulation. In addition to the choice of C_{fly}, the small output voltage and loading of the converter play a role in reducing the total efficiency of the converter below what is normally expected from regular switching mode design (~80%) [8].

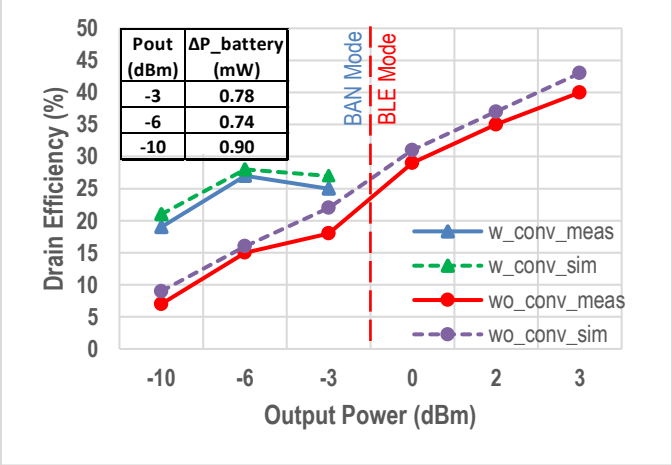

Fig. 6. Simulated and measured drain efficiency for BLE and BAN modes

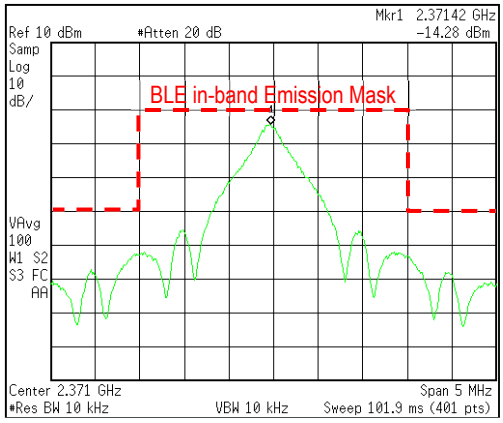

Fig. 7. Power spectrum of the transmitted signal with BLE standard mask

Since the output power is proportional to the square of the supply voltage, the DC-DC converter output voltage of 0.5V to 0.3V covers the output power range of −3dBm to −10dBm. For a better comparison, the effective drain efficiency of the transmitter with the DC-DC converter is measured and plotted alongside that of the conventional design in which the supply is fixed and the number of parallel PA units is varied (Fig. 6). The red plot shows the conventional design when the output power is varied from 3dBm to −10dBm. Due to increasingly larger switch resistance, the efficiency drops from 40% to 7%. Using the converter, the effective drain efficiency improves significantly by as much as 3× at −10dBm. The efficiency is slightly worse at −3dBm due to lower converter efficiency as the output voltage deviates from VDD/2. The absolute power saved from the battery are also shown in Fig. 6. Over 0.9mW saving at −10dBm is significant for BAN applications where the rest of the transceiver system burns less than 1mW.

The power spectrum of the signal meeting the BLE in-band emission mask is shown in Fig. 7. The out-of-band (OOB) emission mask is dominated by the second harmonic (HD2) caused by the LO duty cycle imbalance. Using PMOS/NMOS transistors' programmable bias points, the LO duty cycle can be corrected to improve the HD2. HD2 was measured at −52dBm which meets the BLE standard OOB mask requirement of −30dBm. The multi-mode transmitter performance is compared with that of the state-of-the-art BLE radios in Table I. While delivering competetive performance in high power mode, the trasmitter efficiency and power consumption is significantly better than state-of-the-art in the low power mode, leading to the best figure of merit at −10dBm.

VI. Conclusion

An ultra-low power integrated multi-mode transmitter is presented for both BLE and BAN applications. The transmitter includes a compact PLL whose VCO operates at twice the carrier frequency to eliminate the PA pulling. The proposed PA supply scaling using a fully integrated DC-DC converter is shown to improve the efficiency of the class-D PA efficiency at low output powers (~3×) while showing comparable performance with the state-of-the-art in high power mode. The transmitter consumes 1.6mW at −10dBm output power, which to the best of our knowledge, is the lowest reported power among the transceivers published in the literature.

Table 1. Performance Summary of State-Of-The-Art

Reference	[1]	[2]	[3]	[4]	This Work
Technology	55nm CMOS	40nm CMOS	40nm CMOS	28nm CMOS	40nm CMOS
PA Class	D	D	D	E/F_2	D
Supply Voltage (V)	0.9-3.3	1.1	1	1	1.1
On-chip matching network	Yes	Yes	Yes	Yes	Yes
PLL Integrated PN(°)	N/A	N/A	N/A	0.87	0.83
PN @ 3MHz	N/A	N/A	N/A	N/A	-119.4
TX max P_{OUT} (dBm)	2.3	0	-2	3	4
P_{DC}(mW) @ 0dBm	10.1	7.7	4.2*	3.6	4.5
P_{DC}(mW) @ −10dBm	8.8**	5.4**	2.7**	2.2**	1.6
Chip Area(mm²)	2.9	1.1	1.3	1.84	0.7 (TX)
HD2 (dBm)	-54	-52	-49	N/A	-52
TXFOM* @ 0dBm**	-74.0	-73.1	-72.8	N/A	-75.5
TXFOM @ −10dBm	-74.5	-74.7	-74.6	N/A	-80.0

*at −2dBm **Estimated by interpolation ***TX_FOM=HD2+10log(P_{DC}) [2]

Acknowledgement

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