A 219-to-231 GHz Frequency-Multiplier-Based VCO With ∼3% Peak DC-to-RF Efficiency in 65-nm CMOS

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***Abstract*— Signal sources at mm-wave and (sub-)terahertz frequencies in CMOS can be classified into two broad categories: harmonic oscillators and oscillators that are based on the frequency multiplication of fundamental sources. This paper shows that frequency-multiplier-based sources potentially have a higher dc-to-RF efficiency than do the popular harmonic oscillators in 65-nm CMOS. To improve the power efficiency of CMOS signal sources that operate near or above the cutoff frequency of the device, design factors including the harmonic current efficiency, the effective output conductance, and the passive losses should be carefully tailored. An architecture is proposed in which: 1) the core voltage-controlled oscillator is optimized to efficiently generate a strong fundamental harmonic; 2) separate class-C frequency doublers are utilized to decouple fundamental signal generation and harmonic extraction and to reduce conductance loss; and 3) doubler circuits are separately optimized to simplify the output matching and power combining network, and hence avoid long and lossy transmission lines. A circuit prototype shows a measured peak output power and dc-to-RF efficiency of 3 dBm and 2.95%, respectively.**

***Index Terms*— Coupled oscillators, frequency multiplier, harmonic extraction, harmonic oscillator, mm-wave, terahertz.**

I. Introduction

CMOS promises a low cost, portable platform for a variety of mm-wave and (sub-)THz applications such as medical imaging, noninvasive industrial testing, spectroscopy, and high-data-rate wireless communications [1]. However, efficient power generation at these high frequencies in bulk CMOS processes faces daunting challenges on several fronts: 1) such frequencies are near or above the unity power gain frequency $f_{\max}$ of the transistors; 2) high-frequency loss mechanisms such as substrate loss, skin, and proximity effects deteriorate the quality factor of passive components; and 3) CMOS scaling, though increasing the $f_{\max}$ of MOS transistors, reduces the maximum tolerable signal swing due to lower supply voltage (V_{DD}). To overcome the limited power gain of the device in CMOS technology, device nonlinearity is usually utilized to generate power around the harmonic components. DC-to-RF power efficiency η_p, defined as the output power at the desired RF component to the dc power consumed, is of prime importance for battery-powered systems. Different circuit techniques for more efficient power extraction from a transistor at these frequencies have been developed recently [2]–[13], and η_p for bulk CMOS voltage-controlled oscillators (VCOs) operating near or above $f_{\max}$ is slowly improving (Fig. 1).

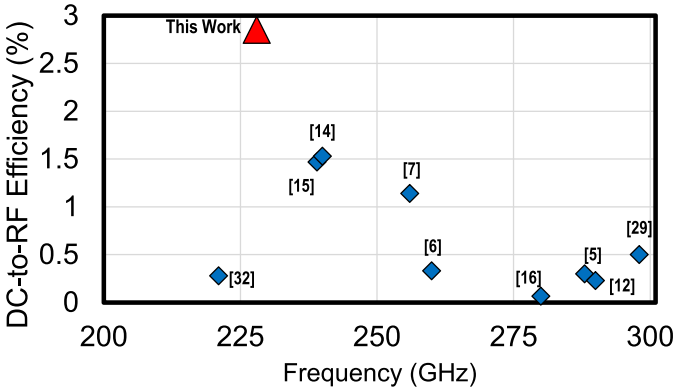

Fig. 1. DC-to-RF efficiency of the recently published VCO with output frequency beyond 200 GHz implemented in CMOS technologies.

Signal sources based on harmonic power extraction leverage either harmonic oscillators or frequency multipliers. Harmonic oscillators, shown in Fig. 2(a), contain active device(s) (M_1) that are simultaneously responsible for providing the power to sustain the oscillation at the fundamental f_0 as well as the desired harmonic, nf_0. The feedback network for oscillation at f_0 is represented by the Y-parameter matrix, $[Y_p]$, and the harmonic output at nf_0 is extracted from the output with a matching network tuned at nf_0. For example, a $2f_0$ component can be extracted at the center-tap of a push–push cross-coupled oscillator [10] using a matching network tuned at $2f_0$, or a $3f_0$ component can be extracted from a triple-push oscillator [4]. Harmonic oscillators with high output power and a good η_p

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are the subject of active research [4]–[12], [14], [16], as shown in Fig. 1. However, higher η_p still remains to be achieved. A frequency-multiplier-based source [Fig. 2(b)], on the other hand, uses an active device (M_1) for sustaining oscillation only at f_0, and uses another active device (M_2) as a non-linear harmonic extractor to give the desired output at nf_0. Recent examples of CMOS frequency multipliers, without integrated fundamental sources, have achieved high output power and high harmonic efficiencies [17]–[20]. Unfortunately, those CMOS sources which have integrated both the fundamental oscillator and the multiplier to efficiently generate harmonic power near or above $f_{\max}$ [2], [21] have not achieved comparable η_p.

To provide a high η_p, the fundamental source and the frequency multiplier must be co-designed and co-optimized together. In this paper, we discuss and compare challenges to design high-efficiency (sub-)THz sources in bulk CMOS processes for each of the above-mentioned method. Optimum conditions to efficiently extract harmonic power (near or above $f_{\max}$) from a MOS transistor are described in Section II, and then impediments to fulfill such conditions for harmonic oscillators are explained in Section III. Multiplier-based sources are then described in Section IV, where it is shown that they can achieve higher overall η_p through optimal co-design and loss minimization, even with additional active stages in comparison to harmonic oscillators. Next, a 219-to-231 GHz multiplier-based source with 2.95% peak dc-to-RF efficiency and 3-dBm peak output power is introduced in Section V. Implemented in a 65-nm CMOS process, in the proposed architecture, four fundamental oscillator cores are injection-locked in-phase together at f_0. Each fundamental oscillator drives a class-C frequency doubler. The output power of these four doublers are combined and matched to the output. Section VI presents the measurement results for the proposed source and compares its performance with other state-of-the-art CMOS oscillators.

II. Conditions for High-Efficiency (Sub-)THz Power Generation in CMOS

A. Conditions for Optimum Fundamental Oscillation

In [4] and [6], optimum conditions for voltage gain ($K = |V_2/V_1|$) and phase ($\varphi = \angle V_2 - \angle V_1$) between the ports of an active two-port network are derived that maximize the net fundamental power generated by the transistor. In harmonic oscillators [Fig. 2(a)], there is no external load (e.g., buffer) to the fundamental signal at f_0 and hence, in the steady state, the fundamental power generated by the active device (P_1) is exactly equal to the fundamental power dissipated in the passive peripheral (P_{passive}). To excite transistor's non-linearity and the harmonic power, usually, it is desirable to increase the gate and drain voltage swings. As voltage swings approach V_{DD}, the active device enters the deep triode region, internal loss increases, P_1 decreases, and eventually, in the steady state, P_1 equals P_{passive}. Assuming that the passive circuit is linear, P_{passive} increases quadratically with the voltage swing. Thus, if the optimum conditions for fundamental power generation are fulfilled, the oscillation sustains at higher voltage swings and hence generates more harmonic power. In other words, in harmonic oscillators, optimum condition for fundamental power generation is *necessary*, but not sufficient, condition to maximize the harmonic power. The transistor sizing and the passive feedback network should be designed such that $K = K_{\text{opt}}$ and $\varphi = \varphi_{\text{opt}}$, and the net power delivered by the transistor at f_0 equals the power dissipated in the passive peripheral circuits at f_0. The optimum phase condition is [4]

$$\varphi_{\text{opt}} = \pi - \angle\left(Y_{12} + Y_{21}^*\right) \tag{1}$$

where, Y_{ij} $(i, j = 1, 2)$ are Y-parameters of the transistor. Under this condition, the maximum power generated at the fundamental harmonic will be [4]

$$P_{\text{out,max}} = \frac{A_g^2}{2}\left(-G_{11} - K_{\text{opt}}^2 G_{22} + K_{\text{opt}}\left|Y_{12} + Y_{21}^*\right|\right) \tag{2}$$

where, G_{ij} denotes the real part of Y_{ij}, and A_g is the fundamental voltage swing at the gate. By using the high-frequency transistor model shown in Fig. 3 [22], [23], Y-parameters of the transistor can be calculated as below

$$Y_{11} \cong R_G(C_{\text{gs}} + C_{\text{gd}})^2\omega^2 + j(C_{\text{gs}} + C_{\text{gd}})\omega \tag{3}$$

$$Y_{12} \cong -R_G C_{\text{gd}}(C_{\text{gs}} + C_{\text{gd}})\omega^2 - jC_{\text{gd}}\omega \tag{4}$$

$$Y_{21} \cong G_m - R_G C_{\text{gd}}(C_{\text{gs}} + C_{\text{gd}})\omega^2 - j(G_m R_G(C_{\text{gs}}+C_{\text{gd}}) + C_{\text{gd}} + C_m)\omega \tag{5}$$

$$Y_{22} \cong G_{\text{DS}} + G_m R_G^2 C_{\text{gd}}(C_{\text{gs}} + C_{\text{gd}})\omega^2 + R_G C_{\text{gd}}^2\omega^2 + (R_{\text{db}} + R_{\text{bb}})C_{\text{db}}^2\omega^2 + j(C_{\text{ds}} + C_{\text{gd}} + C_{\text{db}})\omega \tag{6}$$

where, C_m is the device *transcapacitance* which captures the different effects of the drain and the gate on each other in terms of charging currents [23]. In deriving these formulas, we have assumed that at the frequency of interest, $(R_G(C_{\text{gs}} + C_{\text{gd}})\omega)^2 \ll 1$, and R_s, R_d, L_g, L_s, L_d are negligible. Also, the impacts of R_{sb} and C_{sb} are neglected. Using (1), (4), and (5) we have

$$\varphi_{\text{opt}} \cong \pi - \tan^{-1}\left(\frac{G_m R_G(C_{\text{gs}} + C_{\text{gd}})\omega + C_m\omega}{G_m - 2R_G C_{\text{gd}}(C_{\text{gs}} + C_{\text{gd}})\omega^2}\right) \tag{7}$$

$$\cong \pi - \left(R_G(C_{\text{gs}} + C_{\text{gd}})\omega + \frac{C_m\omega}{G_m}\right). \tag{8}$$

Equation (8) presents a simple expression to design the passive network, where the parameters in the right hand side of (8) can be readily obtained using a dc operating point simulation. Fig. 4 shows that the simulated φ_{opt} matches well with the approximations obtained using (7) and (8). Using (2)–(6), assuming $G_m \gg R_G$ $((C_{\text{gs}} + C_{\text{gd}})\omega)^2$ and $G_m \gg C_m\omega$, $P_{\text{out,max}}$ can be approximated as

$$P_{\text{out,max}} \cong \frac{A_g^2}{2}\left(G_m - K_{\text{opt}}^2 G_{\text{DS}}\right) - \frac{A_g^2\omega^2}{2} \times \left(R_G(C_{\text{gs}}+C_{\text{gd}})^2 + K_{\text{opt}}^2 R_G C_{\text{gd}}^2\left(1 + \frac{G_m R_G(C_{\text{gs}} + C_{\text{gd}})}{C_{\text{gd}}}\right) + K_{\text{opt}}^2(R_{\text{db}} + R_{\text{bb}})C_{\text{db}}^2\right). \tag{9}$$

The first parenthesis in (9) is the frequency independent part of $P_{\text{out,max}}$. As A_g increases, $P_{\text{out,max}}$ increases first. But beyond

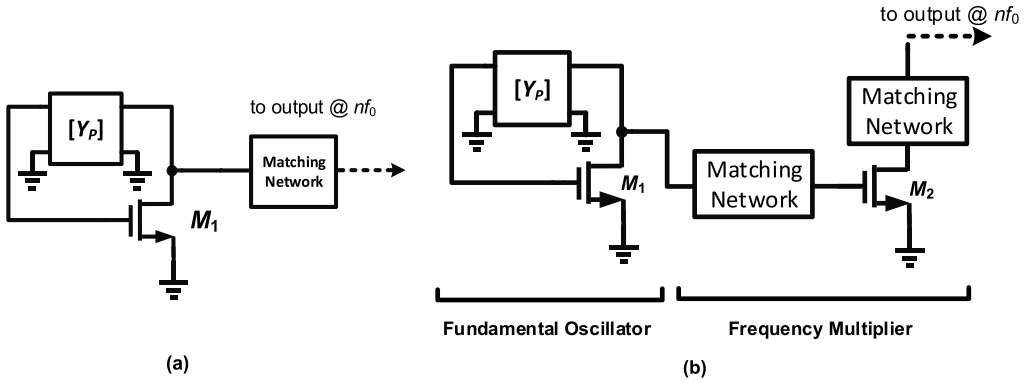

Fig. 2. Generic representation of (a) harmonic oscillator and (b) frequency-multiplier-based source.

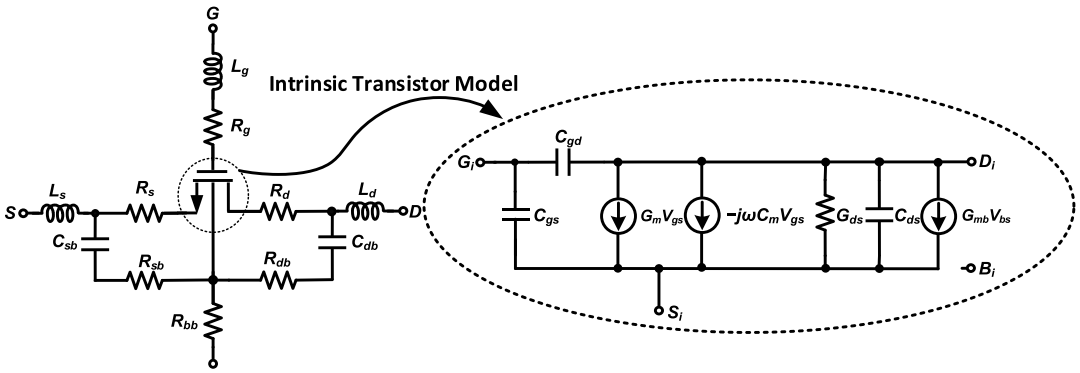

Fig. 3. High frequency, small-signal transistor model. Subscript i represent the intrinsic nodes.

a certain threshold, as A_g increases, the transistor operates in the triode region for greater portion of the oscillation period, the effective G_m degrades, the effective $G_{\rm DS}$ increases and hence $P_{\rm out,max}$ drops. $P_{\rm out,max}$ also degrades with increase in frequency because the power dissipation at the gate (due to R_G) and at the extrinsic part of the transistor (due to $R_{\rm db}$ and $R_{\rm bb}$) rises quadratically with the frequency. Therefore, careful layout of the transistor is important to minimize R_G.

B. Conditions for Efficient Harmonic Power Generation

Consider a cross-coupled pair as shown in Fig. 5. When operating as a push–push oscillator, the resonance circuit (not shown) attenuates higher voltage harmonics so that $v_g(t)$ and $v_d(t)$ of the transistors can be approximated with their fundamental components. At a specific harmonic, a transistor operating under large-signal time-varying regime may be modeled by an equivalent circuit[1] [6]. The available output power of this source is

$$P_{{\rm av},n} = I_{s,n}^2/8G_{s,n} \tag{10}$$

where $I_{s,n}$ is the harmonic component of the drain current at nf_0 and $G_{s,n}$ is the effective conductance seen at the drain of the transistor at nf_0. In general, $I_{s,n}$ and $G_{s,n}$ are functions of the gate signal waveform ($v_g(t)$) and the drain signal waveform ($v_d(t)$). Therefore, $I_{s,n}$ and $G_{s,n}$ will be functions of gate and drain signal amplitudes (A_g and A_d, respectively), drain to gate phase difference (φ), gate bias voltage ($V_{g,\rm dc}$), and operating frequency (f_0). Both $I_{s,n}$ and $G_{s,n}$ can be calculated using harmonic balance simulations. The dc power consumption of the transistor is $P_{\rm dc} = I_{\rm dc} \times V_{\rm DD}$, where $I_{\rm dc}$

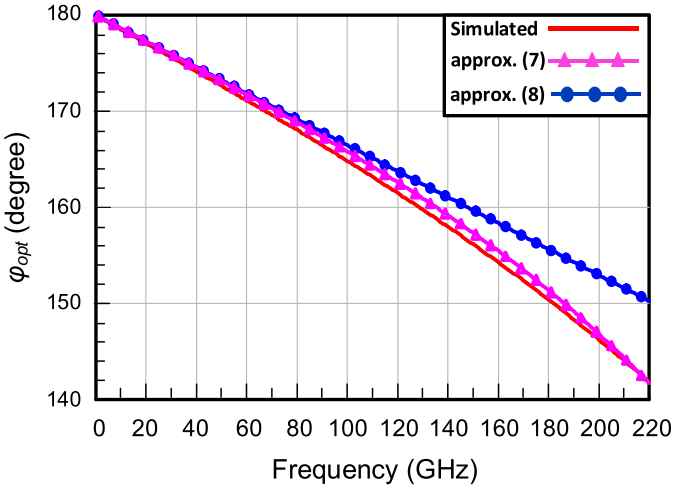

Fig. 4. Simulated (red solid line) and calculated $\varphi_{\rm opt}$ for a 15×1 μm/60 nm NMOS device with $g_m = 20$ mA/V, $R_G = 14.8$ Ω, $C_m = 2.6$ fF, $C_{\rm gs} = 11.8$ fF, and $C_{\rm gd} = 7.4$ fF. The simulated $f_{\rm max}$ for the transistor biased at ($V_{\rm DS,dc}$, $V_{\rm GS,dc}$) = (1.2, 1.2 V) is 233 GHz.

[1]In this model, the impact of the presence of nth harmonic on $I_{s,n}$ and $G_{s,n}$ is not included. For the range of frequencies of our interest, nf_0 falls near or above the device $f_{\rm max}$, and therefore the above approximation usually provides an acceptable estimation for $P_{{\rm av},n}$.

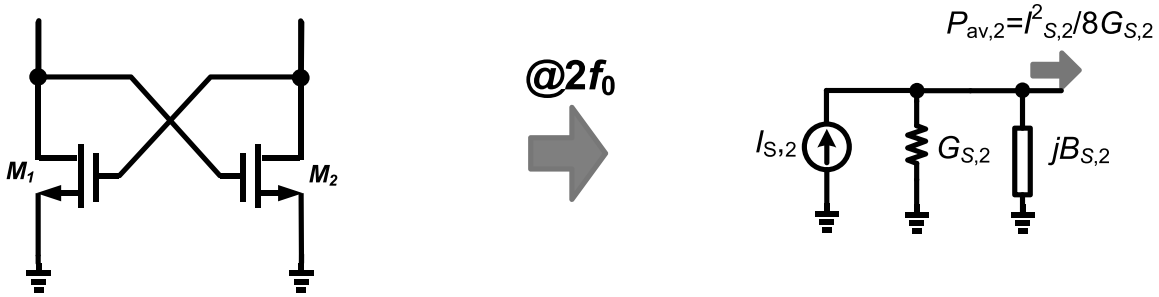

Fig. 5. Cross-coupled pair used in push–push oscillator and its equivalent circuit at a specific harmonic ($2f_0$).

is the transistor dc current. The dc-to-nf_0 power efficiency of the device is written as

$$\eta_{P,n} = \frac{P_{\text{av},n}}{P_{\text{dc}}} = \frac{\eta_{I,n}^2}{8G_{s,n}} \times \frac{I_{\text{dc}}}{V_{\text{DD}}} \tag{11}$$

where $\eta_{I,n} = I_{s,n}/I_{\text{dc}}$ is the drain current efficiency at nf_0. To improve $\eta_{p,n}$ for a specific power consumption, one should increase $\eta_{I,n}$ *and simultaneously* decrease $G_{s,n}$.

III. Challenges in CMOS Harmonic Oscillators

Unfortunately, in harmonic oscillators, $\eta_{I,n}$ and $G_{s,n}$ cannot be optimized simultaneously. In this Section, we first consider a push–push oscillator, and then extend our discussion to a generic harmonic oscillator.

A. Conventional Push–Push Oscillator

Referring to the Section II-A, in conventional push–push oscillator, it can be shown that the optimum phase condition does not hold, because drain to gate phase difference is equal to 180°. Therefore, the necessary condition for efficient harmonic extraction is not fulfilled. Next, we investigate $\eta_{I,n}$ and $G_{s,n}$. Consider a simulation setup for the cross-coupled pair shown in Fig. 6(a), where the drains of the transistors M_1 and M_2 are set to $V_{\text{DD}} = 1.2$ V and superimposed with two sinusoidal voltage sources with opposite phases at $f_0 = 110$ GHz and voltage swing of A. In such a push–push oscillator [10], as oscillation amplitude rises, $I_{s,2}$ and $\eta_{I,2}$ increase [Fig. 6(b)], however, large voltage swings at the gate and drain nodes push the transistor into the deep-triode region, increasing the output conductance at $2f_0$, namely, $G_{s,2}$. On the other hand, the second-harmonic power generated at the drain node is partially dissipated at the gate resistance (R_G), because the drain node is cross connected to the gate of the transistor pair. Moreover, in push–push architectures, the device transconductance (G_m) affects $G_{s,2}$. Indeed, at even harmonics, each transistor in the cross-coupled pair can be considered as a diode-connected device. Neglecting the parasitic capacitance of the device, $G_{s,2}$ will be equal to $G_m + G_{\text{DS}}$ [6]. Increasing effective G_m to achieve a higher oscillation amplitude and to improve $I_{s,2}$ and $\eta_{I,2}$ inevitably results in higher $G_{s,2}$ and hence, lowers second-harmonic power. As a result, according to (10) and (11), both $P_{\text{av},2}$ and $\eta_{p,2}$ degrades [Fig. 6(c)]. In other words, there is a fundamental tradeoff between power generation at the fundamental and at a higher harmonic frequency.

In Fig. 6(c), as A approaches V_{DD} the net power generated at fundamental reduces and eventually, at $A = 1.05$ V, it crosses 0 mW. Beyond this point, though $\eta_{p,2}$ increases significantly, no oscillations are possible because the cross-coupled pair is unable to deliver any power at the fundamental. Consequently, *neglecting all passive losses*, the maximum achievable $\eta_{p,2}$ (i.e., at $A = 1.05$ V) in this 65-nm CMOS technology for the push–push oscillator is about 1.3% at 220 GHz. Repeating simulations for different transistor widths indicates that $\eta_{p,2}$ does not change noticeably with the device dimensions.

An elegant solution to mitigate the impact of G_m is proposed in [6] (self-feeding oscillator) where the feedback between the gate and drain nodes at $2f_0$ is broken by exploiting a quarter-wavelength transmission line (T-line). Although the impact of G_m on $G_{s,2}$ is alleviated in self-feeding oscillator, the gate node still experiences harmonic voltage component at $2f_0$ leading to harmonic loss at the gate due to R_G. More importantly, due to the large fundamental voltage swing at the drain node, the influence of G_{DS} on $G_{s,2}$ still persists.

Another factor affecting both the output power and η_p is the loss in the passive components. To achieve the desired power level at such high frequencies, typically, the harmonic power generated at different oscillator cores are combined. Unfortunately, the loss of the output combining/matching network directly degrades the output power as well as the harmonic power efficiency. For example, consider a push–push (or n-push) structure. In this architecture, the second (or nth)-harmonic generated at the drain of the transistor should inevitably travel along the tank's transmission line (T-line) or inductor to reach node C (Fig. 7), wherein the fundamental power vanishes and the desired harmonic power is combined. Due to the impedance mismatch at node C in Fig. 7, multiple reflections occur which significantly adds loss to the harmonic signal [8], [24]. As an example, in the design proposed in [7], the second-harmonic power generated at the drain of each transistor (at about 250 GHz) should traverse 1.3 mm through T-lines with different characteristic impedances to the output pad. In an optimum design, to avoid this loss, *harmonic power combining should take place right beside the transistor.*

B. Optimum Harmonic Oscillator to Extract $2f_0$

Consider a simulation setup similar to Fig. 6(a) for the generic harmonic oscillator of Fig. 2(a). Assume that two 110-GHz sinusoidal voltage sources are applied again to the

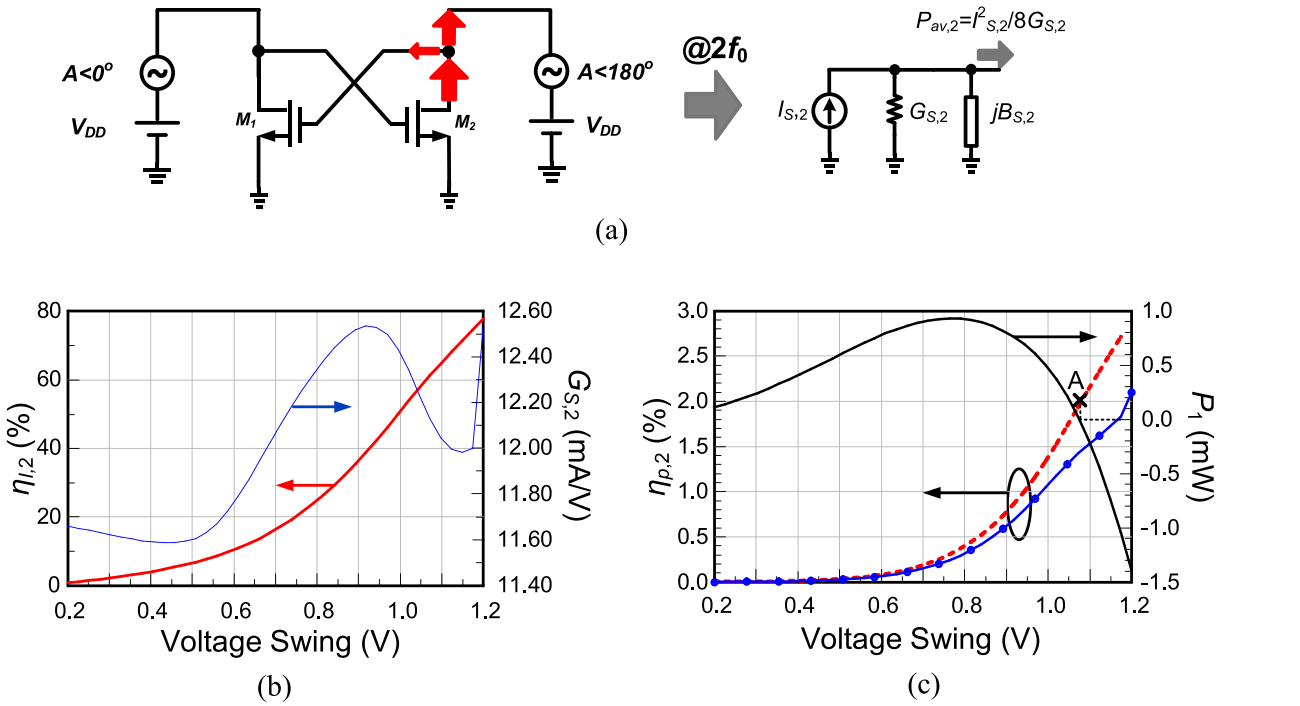

Fig. 6. (a) Simulation setup. (b) $\eta_{I,2}$ and $G_{s,2}$ for a transistor in cross-coupled pair. (c) Total dc to $2f_0$ power efficiency, $\eta_{P,2}$ (circles), drain dc to $2f_0$ power efficiency (dashed curve), and fundamental harmonic power (P_1) generated by the transistor (solid curve).

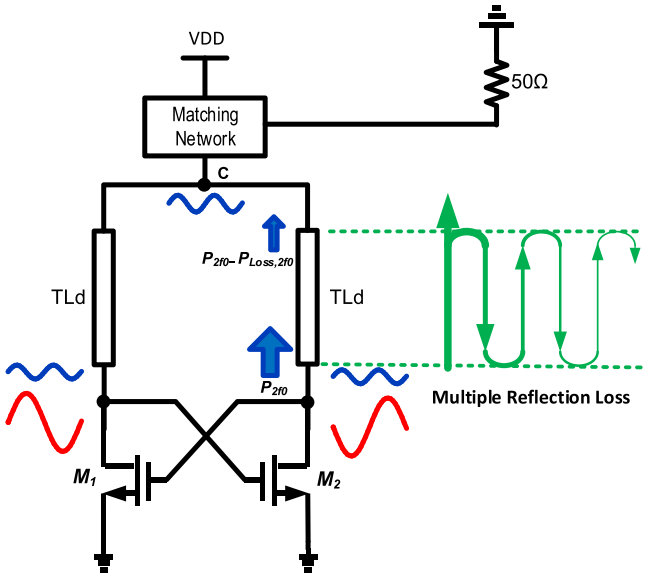

Fig. 7. Second-harmonic power loss in the resonator transmission line of push–push oscillator.

drain and the gate of the NMOS transistor with the same sizing ($W/L = 8\ \mu$m/60 nm) as in Section III-A. If a perfect harmonic isolation is hypothetically assumed between gate and drain terminals, no second-harmonic power is dissipated at the gate. Under this condition, simulations will give an upper limit for $P_{\text{av},2}$ and $\eta_{p,2}$ [6], [8]. The phase of the gate source is set to zero and that of the drain is set to $\varphi_{\text{opt}} = 158°$, which is obtained using the large-signal harmonic-balance simulations. Both the fundamental voltage swings at the gate and drain are swept, $\eta_{I,2}$, $G_{s,2}$, and contours for P_1 and $\eta_{p,2}$ are plotted in Fig. 8(a)–(c), respectively. As the signal swing and dc gate voltage increases toward V_{DD}, $\eta_{p,2}$ increases. Again, neglecting passive power losses, an upper limit for $\eta_{p,2}$ is attained at point A where the contour for $P_1 = 0$ mW touches $\eta_{p,2} = 4.5\%$. However, because of the passive losses (at both f_0 and $2f_0$) and imperfect isolation between the drain and the gate terminals, the reported $\eta_{p,2}$ for CMOS harmonic oscillators proposed to date is much lower than this upper limit. Fig. 8(c) also shows the fundamental tradeoff between the fundamental power generation and the harmonic power generation for the generic harmonic oscillator. As shown in Fig. 8(c), the harmonic power efficiency keeps increasing as A_g and A_d increase. On the other hand, the fundamental power P_1 is maximized at a completely different points and the direction of its variation is also totally different from that of the harmonic power. As evident in Fig. 8(c), passive loss at f_0 results in a lower oscillation amplitude and hence a lower $\eta_{p,2}$ [point B in Fig. 8(c)]. If a wider transistor is used to increase P_1 and the oscillation amplitude, to keep the oscillation frequency constant, inevitably, a smaller tank inductance should be used. Smaller inductors result in higher $P_{\text{passive}}(= A^2/(2LQ\omega))$, if Q is assumed to be constant. Consequently, it again degrades $\eta_{p,2}$.

To summarize, efficient harmonic power generation using harmonic oscillators suffers from the following issues: 1) harmonic power generated at the drain of the transistor is partially dissipated at the gate; 2) increasing the oscillation amplitude to increase $\eta_{I,2}$ can significantly degrade the effective output conductance of the transistor at $2f_0$ (or nf_0) [Fig. 8 (a), (b)]; and 3) the harmonic power generated at the drain of a MOS transistor is significantly attenuated because of insertion loss and multiple reflection loss in the passive network at $2f_0$. The biggest limitation for harmonic oscillators is the fact that

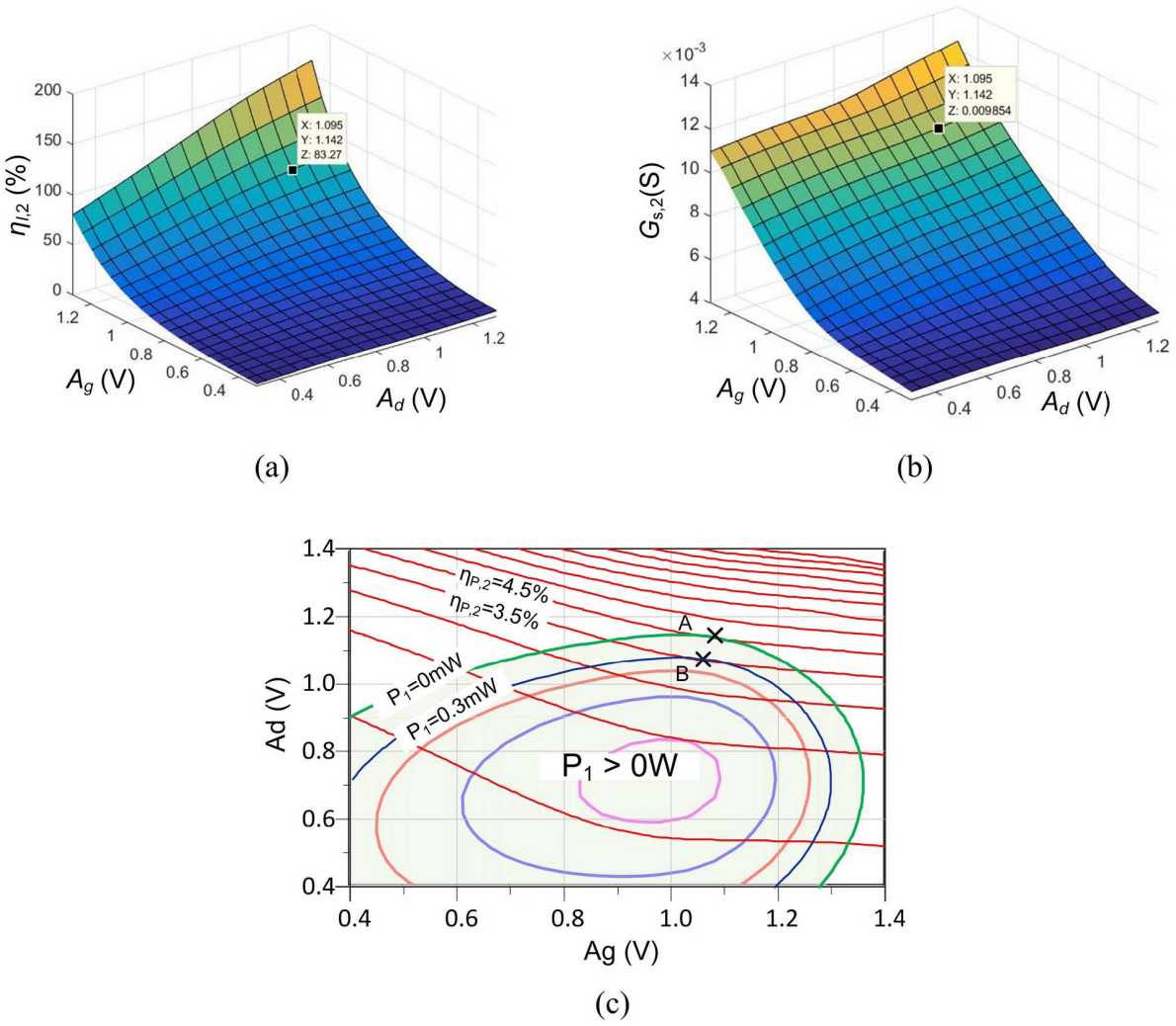

Fig. 8. Contours for (a) $\eta_{I,2}$, (b) $G_{s,2}$, and (c) dc to second-harmonic power efficiency ($\eta_{p,2}$) (step = 1%) and fundamental power (P_1) (step = 0.3 mW) for generic harmonic oscillator. Shaded area shows device activity region.

a single transistor simultaneously generates harmonic power and restores fundamental passive loss.

IV. Frequency-Multiplier-Based Sources in CMOS

The above-mentioned issues of harmonic oscillators can be addressed in multiplier-based signal sources. Consider the generic multiplier-based source shown in Fig. 2(b), where M_2 is used for frequency multiplication. As the drain node of M_2 does not necessarily experience high swing at f_0, M_2 can operate without being pushed into the triode region for large voltage swings at the gate node, and hence $G_{s,2}$ does not degrade. Besides, in comparison to a cross-coupled pair, there is neither a negative feedback from the drain to the gate, nor any harmonic power that is being dissipated at the gate. As a result, there is no severe tradeoff between the harmonic current efficiency $\eta_{I,2}$ and $G_{s,2}$. Furthermore, unlike harmonic oscillators, where both the fundamental power (at f_0) and the harmonic power (at $2f_0$) generated at the drain of the transistor suffers from the loss of the T-line in the core oscillator tank (see Fig. 7), only the fundamental power (at f_0) suffers from such loss here. The harmonic power (at $2f_0$) at the drain of M_2 can be directly delivered to the output matching/combining network. Therefore, a transistor employed in a multiplier can more efficiently extract harmonic power as compared to a transistor used in a harmonic oscillator.

The main drawback of the (sub-)THz multiplier-based signal source is that a separate high-power fundamental signal source is needed to drive the frequency multiplier. The overall η_p of the system will therefore be strongly dependent on the power efficiency of the fundamental oscillator. Next, we quantitatively compare the maximum achievable harmonic power efficiency of the CMOS multiplier-based source to that of the harmonic oscillator.

Consider M_2 used as a frequency doubler in Fig. 2(b) to have a size of $(W/L) = (8\ \mu\text{m}/60\ \text{nm})$ and a 110-GHz sinusoidal source applied to its gate only. The drain terminal is simply connected to the supply voltage. Both the gate dc voltage ($V_{G,\text{dc}}$) and voltage swing (A) are swept, and then $\eta_{I,2}$, $G_{s,2}$, $\eta_{p,2}$, and $P_{\text{av},2}$ are plotted in Fig. 9(a)–(d), respectively. In these simulations, the drain node of M_2 does not see

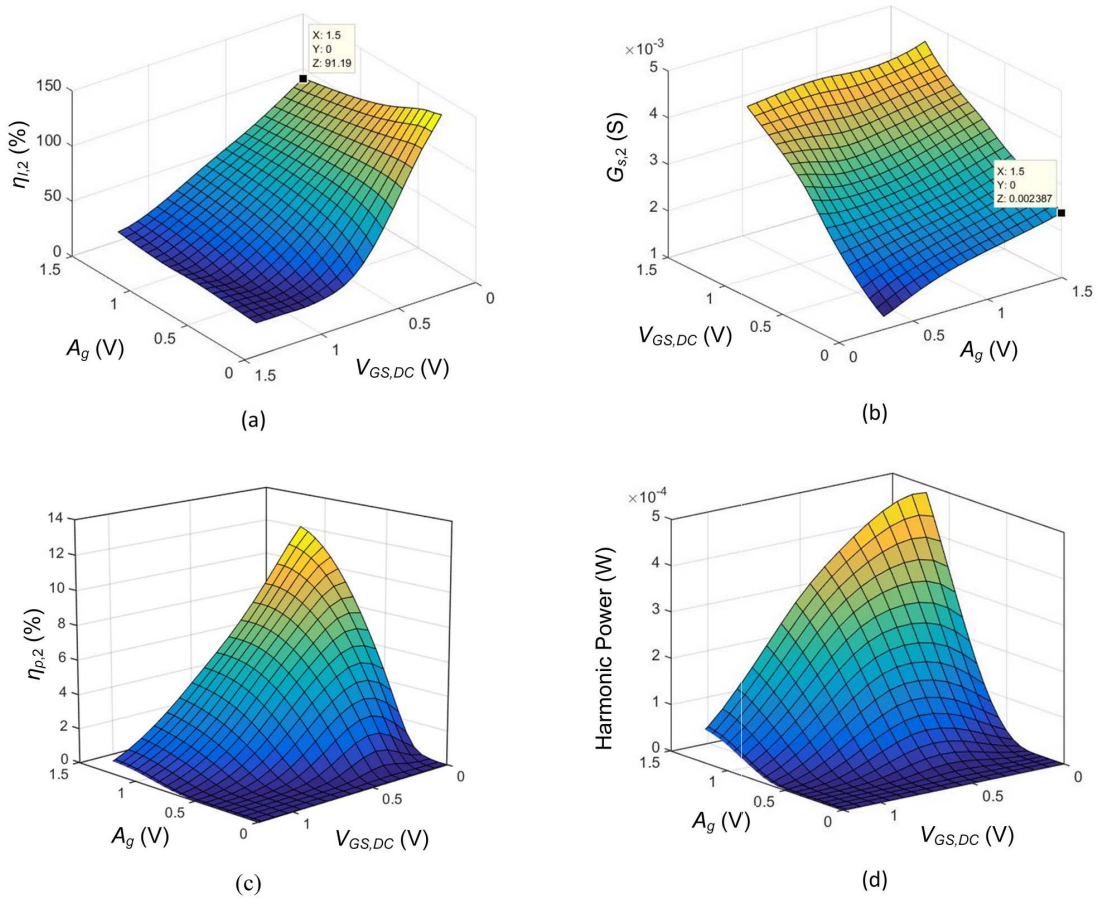

Fig. 9. (a) $\eta_{I,2}$, (b) $G_{s,2}$, (c) $\eta_{p,2}$, and (d) $P_{\mathrm{av},2}$ for the frequency doubler with respect to fundamental gate swing (A_g) and dc level $V_{G,\mathrm{dc}}$.

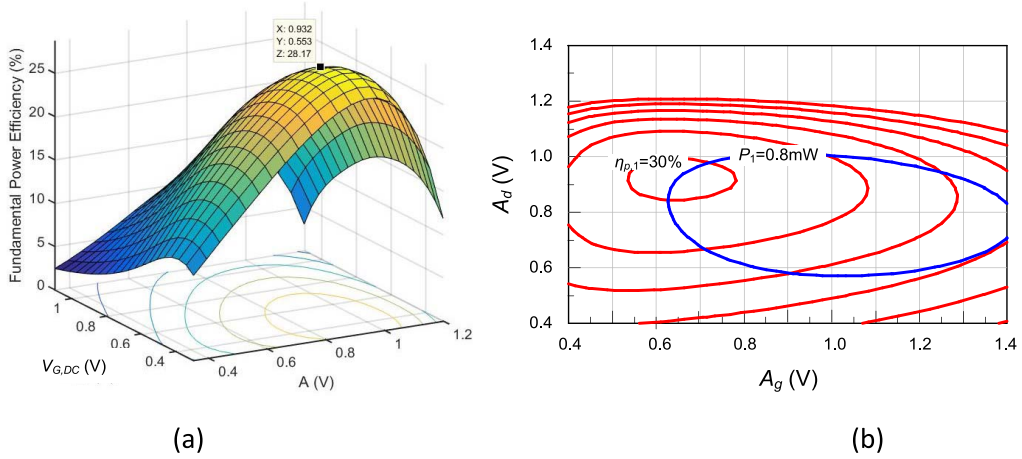

Fig. 10. (a) Fundamental power efficiency plot with respect to $A = A_g = A_d$ and gate dc voltage (V_{dc}). (b) Fundamental power efficiency contours (max = 30% and step = 5%) for core oscillator and $P_1 = 0.8$ mW.

any fundamental swing. As shown in Fig. 9(c) and (d), both P_{out} and $\eta_{p,2}$ are maximized as $V_{G,\mathrm{dc}}$ approaches 0 V. Thus, by choosing $V_{G,\mathrm{dc}} = 0$, the conduction angle of the current waveform is reduced and higher second-harmonic current is generated [Fig. 9(a)]. As shown in Fig. 9(c), $\eta_{p,2}$ can be as high as 12% at ($V_{G,\mathrm{dc}}$, A) = (0, 1.5 V), which is significantly higher than the corresponding upper limit of $\eta_{p,2} = 4.5\%$ for the harmonic oscillator. Near $\eta_{p,2} = 12\%$, $V_{G,\mathrm{dc}} = 0$ V, and therefore, the conduction angle of the doubler transistor is lower than 180° and it is operating in class-C mode. The next step is designing a fundamental oscillator to drive the doubler. The fundamental power that flows into the gate of the doubler transistor M_2 at ($V_{G,\mathrm{dc}}$, A) = (0, 1.2 V), translated into $\eta_{p,2} =$ 11.5% and $P_{\mathrm{av},2} = 320$ μW, is 0.8 mW. The fundamental oscillator should deliver 0.8 mW to the frequency doubler with minimum dc power consumption. To increase $\eta_{p,1}$ for

the fundamental oscillator, we can decrease the $V_{G,\mathrm{dc}}$ of the core transistor [M_1 in Fig. 2(b)], without any consideration of $\eta_{p,2}$. Fig. 10(a) shows simulated $\eta_{p,1}$ with respect to $V_{G,\mathrm{dc}}$ and voltage swing $A = A_d = A_g$ when $\varphi = \varphi_{\mathrm{opt}}$. From Fig. 10, it is evident that around $V_{G,\mathrm{dc}} = 0.5$ V, $\eta_{p,1}$ is maximized. Note that in harmonic oscillators, on the other hand, decreasing $V_{G,\mathrm{dc}}$ while improving $\eta_{p,1}$ degrades $\eta_{p,2}$. To achieve the highest fundamental power and efficiency, φ is set again to φ_{opt} and $V_{G,\mathrm{dc}}$ is reduced to 0.5 V, and $\eta_{p,1}$ contours with respect to A_g and A_d ($A_g \neq A_d$) are plotted in Fig. 10(b). The highest $\eta_{p,1}$ contour that intersects with $P_1 = 0.8$ mW contour gives $\eta_{p,1} = 30\%$. Interestingly, at ($V_{G,\mathrm{opt}}$, φ_{opt}) = (0.55 V,158°) in Fig. 10(a), the transistor delivers a power efficiency of 28% which is more than double of what it delivers in a standard cross-coupled configuration at (V_G, φ) = (1.2 V, 180°). By inspecting Fig. 10, one can conclude that in order to optimize the output power and the power efficiency of the fundamental oscillator, A_g, A_d, φ, and $V_{G,\mathrm{dc}}$ should be carefully tailored. In general, passive circuits embedding the transistor(s) determine the above-mentioned conditions.

The fundamental oscillator consumes 2.66 mW to deliver 0.8-mW power at 110 GHz to the frequency doubler. With $\eta_{p,2} = 11.5\%$ and $P_{\mathrm{av},2} = 320$ μW in the multiplier, the multiplier consumes 2.78 mW, leading to an overall dc power consumption of 5.44 mW and dc-to-RF efficiency of 5.9%. One can therefore conclude that, within the frequency range of our interest in 65-nm CMOS, the oscillator-doubler combination more efficiently extracts $2f_0$ power from dc compared to a harmonic oscillator ($\eta_{p,2} = 4.5\%$).[2] As mentioned earlier, the maximum $\eta_{p,2} = 4.5\%$ for a harmonic oscillator is achieved by assuming perfect harmonic isolation between gate and drain terminals and also by neglecting the passive loss at f_0 and $2f_0$. Due to these facts, in practice, $\eta_{p,2}$ for harmonic oscillators will be significantly lower than this limit. But, in multiplier-based sources, the maximum $\eta_{p,2} = 5.9\%$ is relatively less affected by the passive losses and imperfect harmonic isolation between gate-drain as compared to the harmonic oscillators. Repeating the above procedure for other transistors and harmonic power levels results in a similar conclusion.

V. Proposed 219-to-231 GHz CMOS VCO

A multiplier-based source, being more efficient in generating second-harmonic power at 219-to-231 GHz in the 65-nm CMOS process, is used in the proposed VCO architecture, shown in Fig. 11. The structure comprises of four differential oscillator cores, each oscillating at f_0 (∼110 GHz) and injection locked together to operate in phase at f_0. The oscillator core at the fundamental frequency is designed using the procedure presented in Section IV. The cores are passively coupled together through T-lines (TL_C) based on grounded co-planar waveguides (GCPW) [24]. It should be noted that the TL_C lines are part of resonator and affect the oscillation frequency. This passive coupling scheme does not dissipate additional dc power, and is therefore attractive for overall efficiency. The output of each core feeds an active doubler designed to efficiently extract the second-harmonic ($2f_0$) power by operating in class-C mode. To increase the output power, the harmonic power of the doublers should be combined. As the fundamental differential signals driving the doublers are in phase, the second-harmonic components at the output of the doubler also remain in phase and add to each other constructively, while the fundamental tones vanish. Care must be paid in the layout because any mismatch between cores results in imperfect fundamental tone cancellation and also reduction in output harmonic power. To avoid mismatch, the layout is designed to have four-way symmetry. Coupling N oscillators together reduces the phase noise by $10\log(N)$, therefore, the phase noise of the overall source is 6 dB lower than the phase noise of a single core. The detailed schematic of the proposed VCO is shown in Fig. 12. For the oscillator core, L_G, L_D, L_C, and C_C are chosen such that the optimum condition for voltage swings and phases at the gate and drain terminals are fulfilled. A design procedure to find their optimal values is described in the Appendix. For the cores, as adjacent transistors should operate in opposite phases, RF blocking resistors R_g (∼2 kΩ) have been added to the center-tap of the TL_C to prevent unwanted even-mode oscillation, whose frequency is far below that of the desired differential-mode oscillation at f_0. Simulations show that these resistors slightly improve the power efficiency of the core oscillators. Slow-wave GCPW are used to reduce loss for a given electrical length [29] and their ground planes are implemented using the two lowermost metal layers, represented by the shaded gray areas in Fig. 12. Short T-lines at the gate of the frequency doublers (L_G) perform impedance matching and enhance the signal swing at the gate. Recall from Fig. 9(c) that $\eta_{p,2}$ is highly dependent to the fundamental voltage swing. Indeed, these T-lines boost the fundamental swing from the optimum gate swing for the core oscillator to the optimum input swing for the doublers. The dc bias of the core transistors, $V_{G,\mathrm{dc}}$,

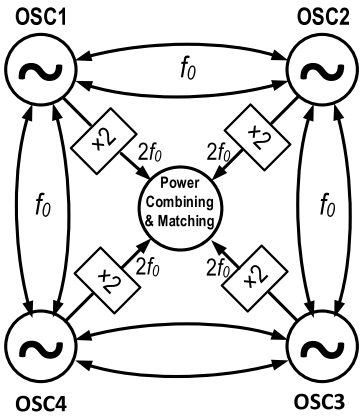

Fig. 11. Proposed VCO architecture.

[2]As mentioned before, the impact of the second harmonic has not been included in our discussion. The presence of the second harmonic voltage at the drain of the transistor can move $P_1 = 0$ contour upward in Fig. 8(c), thereby improving $\eta_{p,2}$ for harmonic oscillators. In case of multiplier-based sources, the presence of the second harmonic components will improve the fundamental power generation efficiency of the core oscillator as well as the harmonic power generation efficiency of the doubler. Thus, the conclusion remains valid even if the impact of the second harmonic components is taken into account.

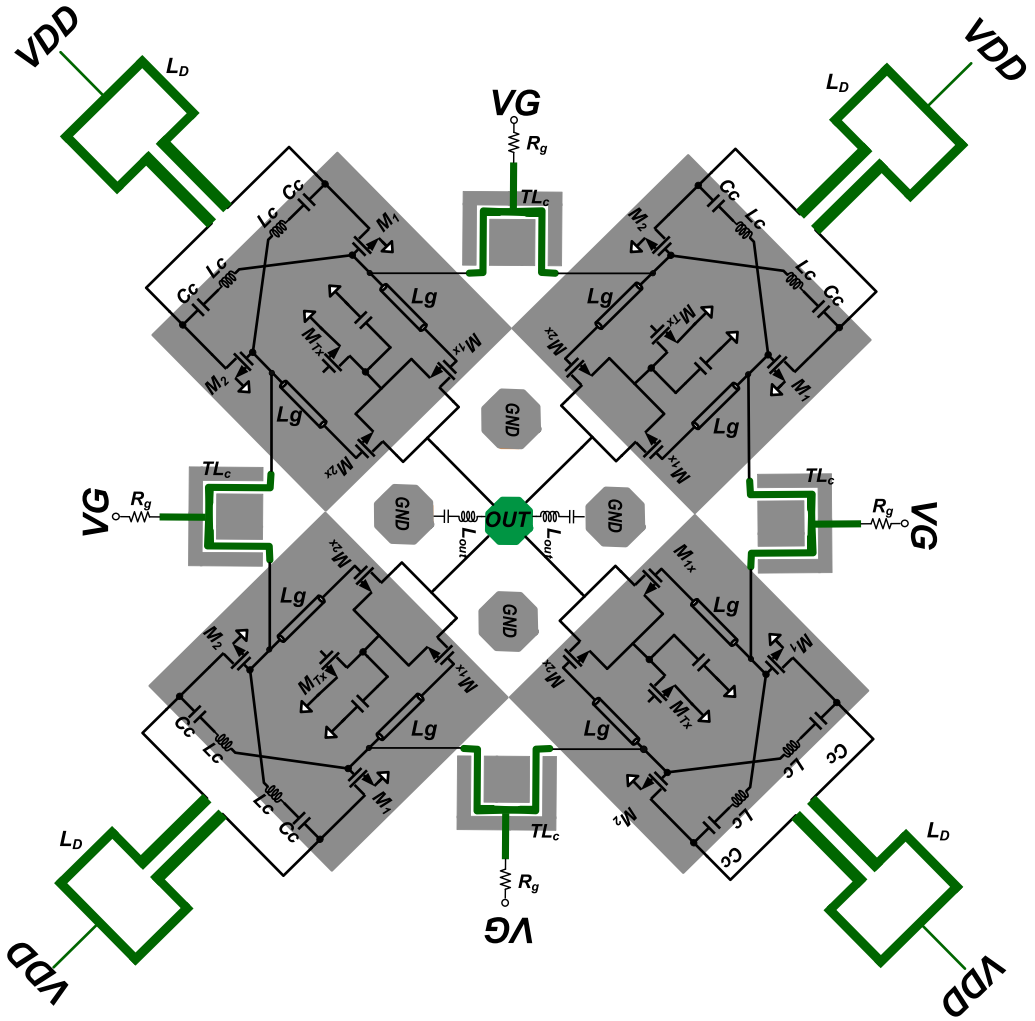

Fig. 12. Detailed schematic of the proposed VCO.

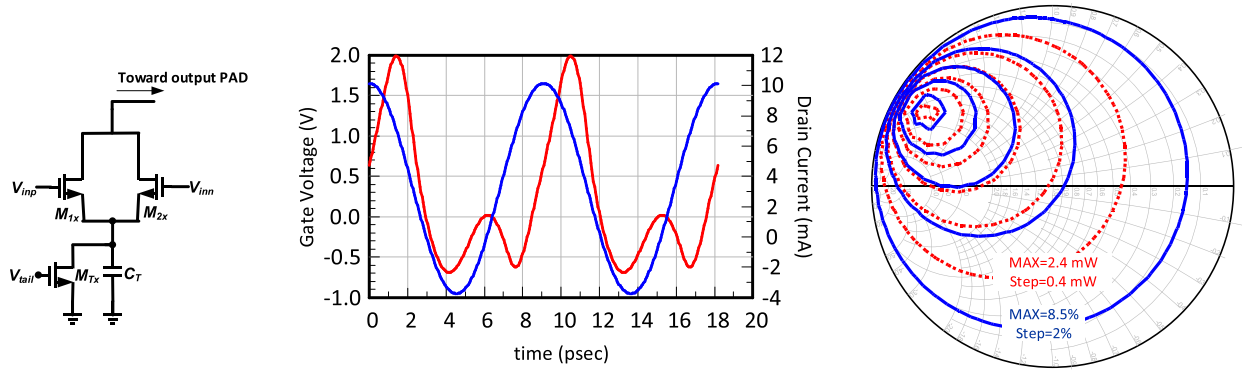

Fig. 13. (a) Frequency doubler, with $W/L = 8$ μm/60 nm for M_{1x} and M_{2x}. (b) Gate voltage and drain current waveforms. (c) Output power (dotted curve) and power efficiency (solid curve) contours for gate signal swing $A = 1.3$ V at 110 GHz for four frequency doublers combined together.

is provided through the center tap of the TL_C lines. Next, we describe the frequency doubler and the tuning scheme for the proposed VCO.

A. Class-C Frequency Doubler

Fig. 13(a) shows the frequency doubler used in the proposed VCO. In this circuit, the differential pair (M_{1x} and M_{2x}), the tail transistor (M_{Tx}) and the large tail capacitor C_T ($\sim$300 fF) form an amplitude peak detector in which the dc value of the common-source node increases as the signal swing at the gate of M_{1x} and M_{2x} increases. The tail capacitor is charged during the oscillation build-up to a voltage level slightly below the input dc voltage of the differential pair. Consequently, conduction angle (ϕ_C) of the drain current

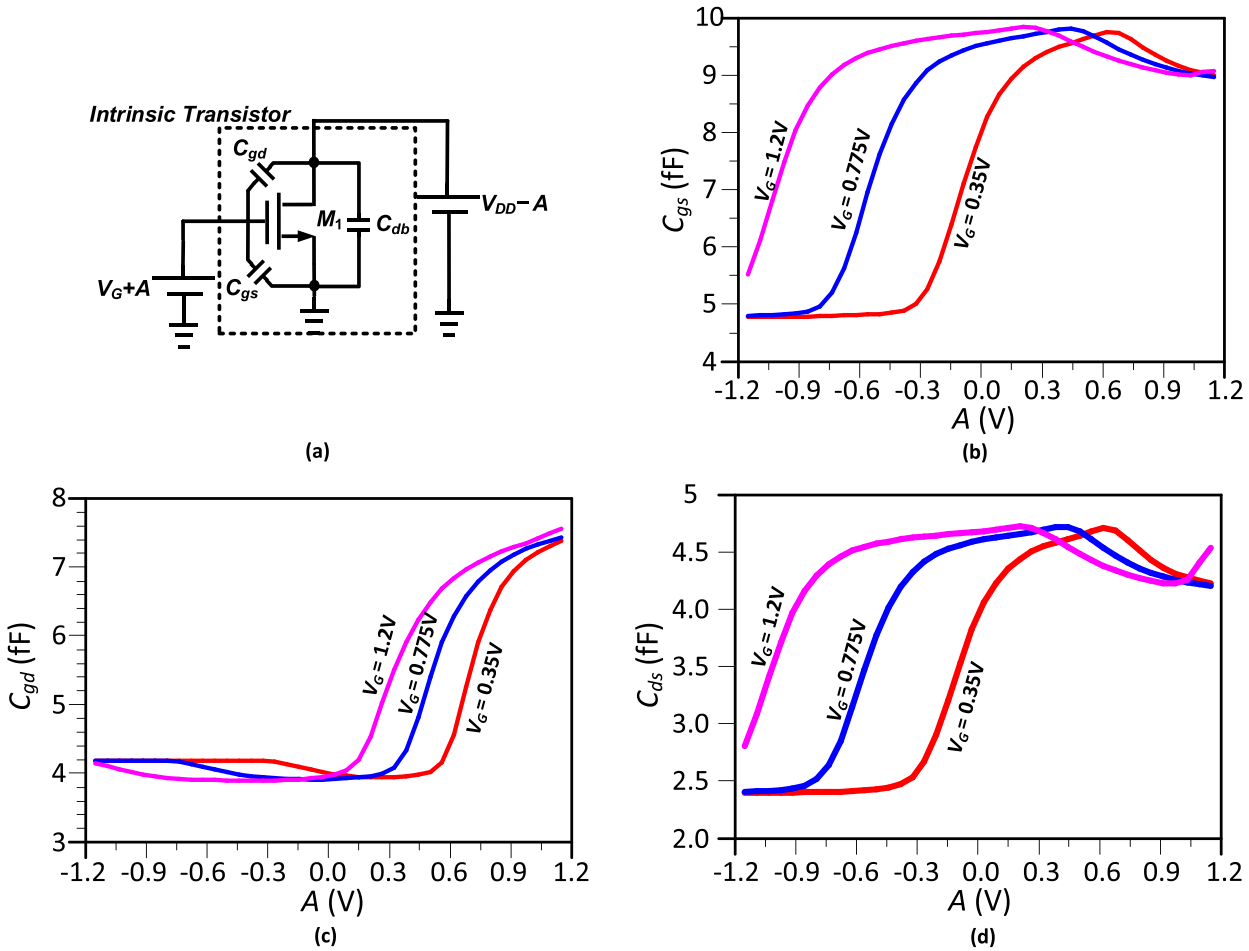

Fig. 14. (a) Parasitic capacitances of a MOS transistor, and different C–V characteristics for (b) $C_{\rm gs}$, (c) $C_{\rm gd}$, and (d) $C_{\rm ds}$, for $V_G = 0.35$, 0.77, and 1.2 V.

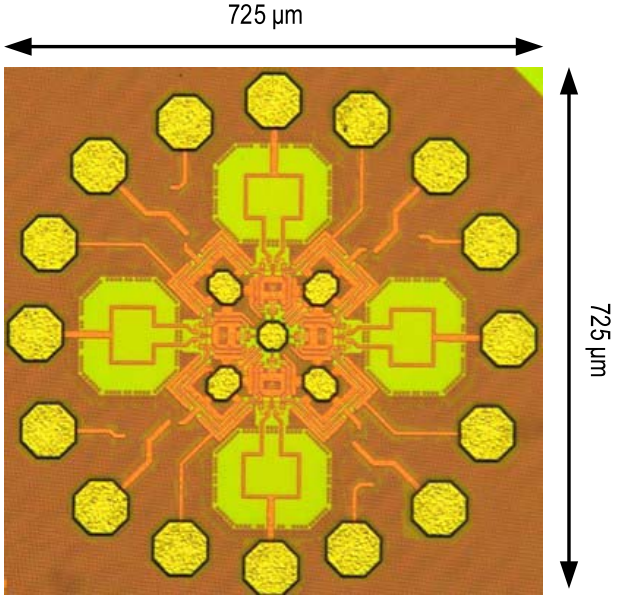

Fig. 15. Chip micrograph.

waveform becomes smaller than π radians, driving the transistors M_{1x} and M_{2x} in class-C mode. Simulated drain current and gate voltages are shown in Fig. 13(b). In this circuit, there is no large fundamental signal swing at the drain node. Thus, transistors operate in the saturation region and their effective output conductance remains at their minimum, which according to (11) maximizes the second-harmonic power generation efficiency. When the multiplier is operating in class-C mode, it can be shown that for a conduction angle of ~75°, $\eta_{I,2}$ could be as high as 100% [25]. If the fundamental swing A at the gate of device increases, the conduction angle decreases and the dc-to-RF efficiency increases. By exploiting a high-frequency transistor model [22] shown in Fig. 3, (6) provides an approximation for the output conductance of the class-C harmonic extractor which can be written as

$$G_{S,2f_0} \cong 2\big(G_{S0} + 4\pi^2 f_0^2\big(R_d(C_{\rm ds} + C_{\rm db})^2 + R_G C_{\rm gd}^2 + (R_{\rm db} + R_{\rm bb})C_{\rm db}^2\big)\big) \quad (12)$$

where, G_{S0} is the effective low-frequency output conductance of a transistor operating in class-C regime, and is approximately equal to $\varphi_C \times g_{\rm ds}/2\pi$. According to (11) and (12), the available power of class-C frequency doubler decreases with increase in operating frequency. Furthermore, R_G should be minimized in layout to reduce the output conductance.

Output power and efficiency contours for the frequency doubler, obtained from load–pull simulations, are shown in Fig. 13(c). To simplify output matching and power

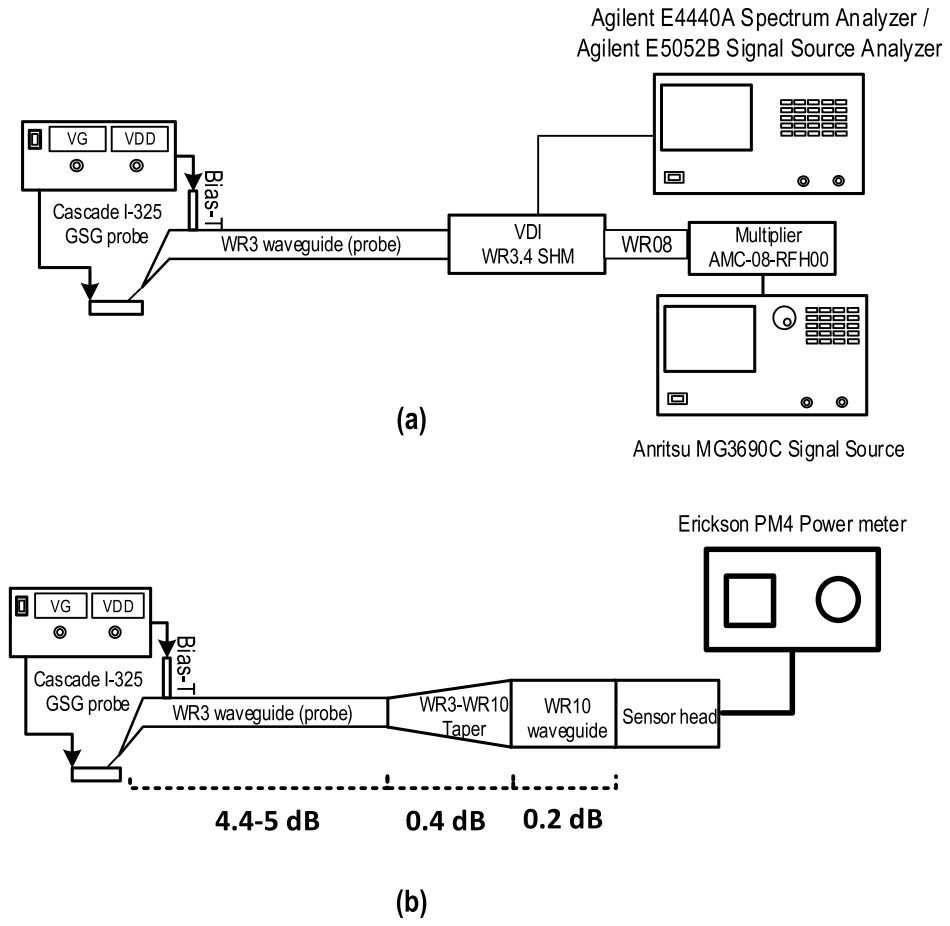

Fig. 16. (a) Frequency, phase noise, and (b) power measurement setups.

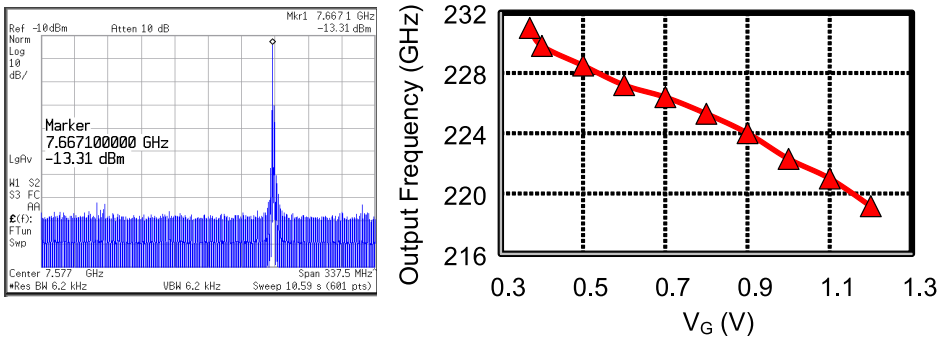

Fig. 17. (a) Measured spectrum for LO input of 13.9 GHz whose 16th harmonic down-converts the RF input of 230.06 to 7.66 GHz. (b) Measured tuning curve.

combining networks, transistors are sized such that all doubler blocks provide 50 Ω matching when combined together, and their capacitances are tuned out using output inductors, L_{out}.

B. Frequency Tuning Scheme

In the proposed design, the use of an explicit varactor is avoided due to their high loss at mm-wave frequencies. MOS parasitic capacitances are instead employed for frequency tuning. Fig. 14 illustrates the change in parasitic capacitances to voltage (C–V) for the three distinct operating regions (cut-off/saturation/triode), which the transistor spans during one oscillation period. As the effective parasitic capacitance depends on the gate dc bias voltage V_G it can be used as the control voltage. One drawback of such intrinsic tuning scheme is that the power efficiency of the source degrades with increasing V_G [refer to Figs. 9 and 10(a)]. This can be remedied in a future design by decoupling the dc bias of

TABLE I

MEASURED PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART DESIGNS OPERATING BETWEEN 200 AND 300 GHz

Reference	[4]	[12]	[6]	[7]	[26]	[27]	[5]	[14]	[28]	[29]	[30]	[31]	This Work
Center Freq. [GHz]	256	288	260	256	222	296	290	239	215	298	247.5	190	225
Tuning Range [%]	NA	1.4[a]	1.4	4.3 (6.5[a])	20%	2.4	4.5	12.5	0.65	1.7	10.5	21	5.33
DC Power [mW]	71	275	800	227	35	67.2	325	18.5	79	235	386	294	68
Peak DC-to-RF Efficiency [%]	0.03	0.3	0.33	1.14	4.5[c]	5.15[d]	0.23	1.47	4.6	0.5	1.3	0.21	2.95
VDD [V]	1.25	1.25	1.2	1.6	1.5	1.4	1.3	1.2	1.6	0.95	1.8/1.2[b]	2.1	1.2
Phase Noise @ 1 MHz [dBc/Hz]	-88	-87	-78	-94	NA	NA	-78	-90	-94.6	-79	-82	-102 @10MHz	-94 @227GHz
Peak Output Power [dBm]	-17	-1.5	0.5	4.1	2	5.4	-1.2	-4.8	5.6	0.9	7.2	-2.1	3
Source Type	Harmonic oscillator	Harmonic oscillator	Harmonic oscillator	Harmonic oscillator	Balanced doubler	Locked Harmonic oscillator	Harmonic oscillator	Harmonic oscillator	Harmonic Oscillator	Harmonic oscillator	Multiplier-Based	Harmonic oscillator	Multiplier-based
Technology	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	90nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS	65 nm CMOS	65nm CMOS	55nm SiGe	130nm BiCMOS	65nm CMOS

a) Including frequency tuning by change of supply voltage.
b) VCO uses a 1.8 V supply and doubler employs a 1.2 V supply voltage.
c) Excluding the DC power consumption of the driving fundamental source.
d) Excluding the DC power consumption of the external locked reference.

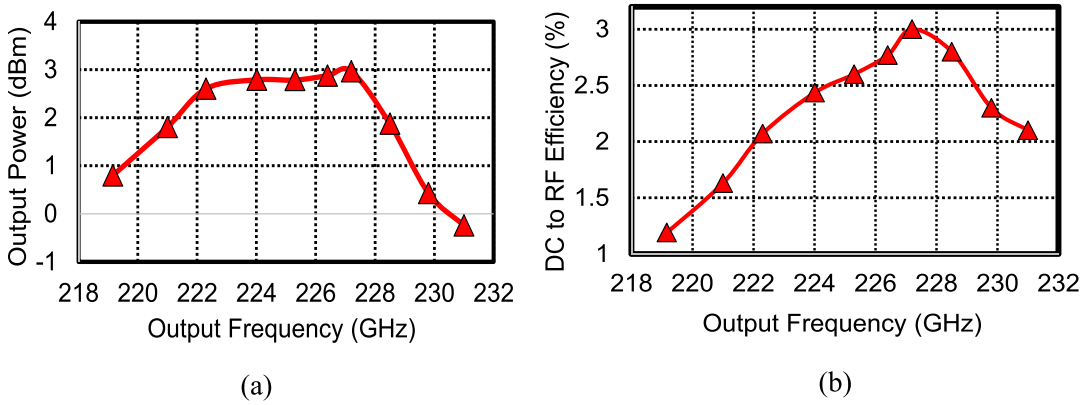

Fig. 18. Measured (a) output power and (b) dc-to-RF efficiency.

the core fundamental oscillator from the frequency doubler. In this way, the gate bias of the core oscillator and the doubler can separately be chosen and hence, overall dc-to-RF efficiency will improve.

VI. MEASUREMENT RESULTS

Fig. 15 shows the micrograph of the chip, implemented in a 65-nm CMOS process with an area of 725×725 μm^2. The output of the VCO is taken near the center of the layout for the purpose of testing this proof-of-concept chip. In real applications, depending on many factors including whether the source should drive an antenna or other circuits, the floorplan of the whole system, the number of coupled cores, the required output power and the layout of the source should be tailored. All passives are carefully simulated using the Sonnet electromagnetic simulator. The ground layer underneath the output signal pad is removed to reduce the parasitic capacitance of the pad from 22 fF to about 13 fF, with 45 μm opening. The parasitic capacitance of the pad and the doubler block is tuned out by adding a short T-line between the signal and ground pads which realizes impedance matching at the output.

Fig. 16(a) shows the experimental setup used for frequency measurement. The output pads of the VCO are connected to a Cascade i325-GSG *infinity* probe with a built-in bias tee that feeds dc voltage to the drain of the doublers. Other dc voltages are provided by wirebonds that connect dc pads to the test printed-circuit board. For frequency measurement

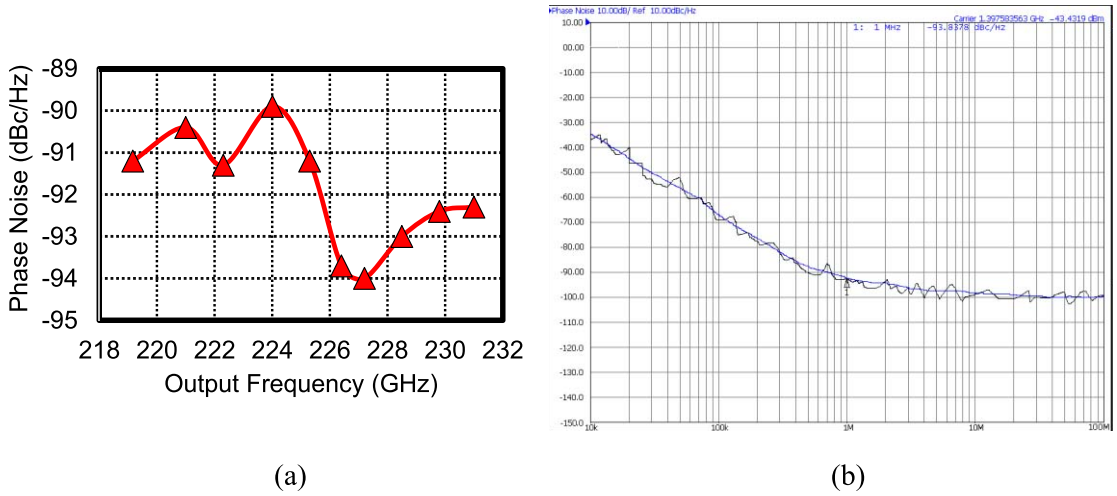

Fig. 19. Measured (a) phase noise at 1-MHz offset, as the oscillation frequency is varied across the tuning range and (b) down converted phase noise plot at the output frequency of 227 GHz downconverted to 1.39 GHz using the 16th harmonic of 14.1-GHz LO input.

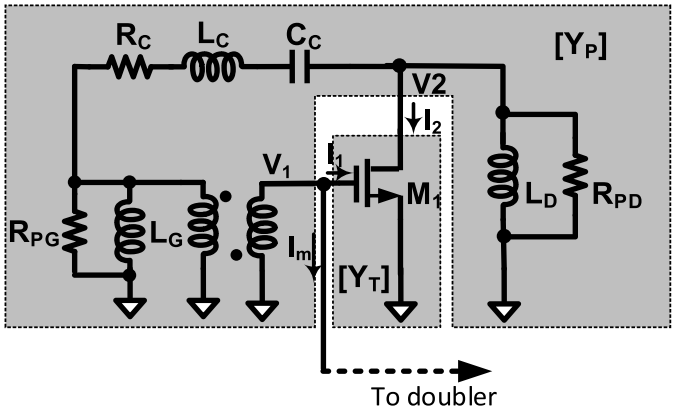

Fig. 20. Equivalent half-circuit of the proposed oscillator at f_0.

purposes, a VDI WR3.4 subharmonic mixer (SHM) is used to down-convert the signal. This SHM mixes the signal at its RF port with the signal at twice the local oscillator (LO) frequency. The LO signal of SHM at 90-to-140 GHz is obtained by multiplying the output signal of the 11.25-to-17.5 GHz signal generator with an 8× frequency multiplier (AMC-08-RFH00). Fig. 17(a) shows the spectrum of the IF signal, obtained through down-conversion by the 16th harmonic of the LO. The tuning range, measured with respect to the V_G is shown in Fig. 17(b). Although the output power may be estimated using the measurement setup of Fig. 16(a), the large non-linearity of the SHM with respect to LO and RF ports renders the estimation of output power inaccurate [19]. In order to correctly measure the output power [4], [5], [7], [9], [14], [19], [26], [28], [30], a power measurement setup incorporating an Erickson PM4 power meter is used, as shown in Fig. 16(b). The symmetry of the source, in conjunction with the band-pass filter characteristic of the WR3 waveguide, ensures that all undesired harmonics are attenuated and the power meter detects the desired harmonic only.

The loss of all measurement setup including probes, tapered waveguides, and connection cables are de-embedded. The measured probe loss is provided by the manufacturer (Cascade Microtech), and it varies between 4.4 to 5 dB within the frequency range of the DUT. The loss of the WR10 waveguide and the WR3-WR10 taper are 0.2 and 0.4 dB, respectively. Fig. 18 shows the measured output power and η_p, with respect to the output frequency. For power measurement at 219 GHz, a setup similar to Fig. 16(b) is used, but with a Cascade i220-GSG probe and a WR5-WR10 taper. As shown, the maximum output power achieved at 227 GHz is about 3 dBm. The variation of the output power is less than 4 dBm within the tuning range. Total dc power consumption varies from 45 to 101 mW by changing V_G. For higher V_G, which results in lower output frequencies, the fundamental voltage swing increases, and therefore the power consumption increases. Since the conduction angle for both the core oscillator and the frequency doubler increases with V_G, their power efficiencies degrade. The peak η_p, is 2.95% and it remains higher than 1% across the tuning range. Phase noise at 1 MHz offset varies from −94 dBc/Hz to −90 dBc/Hz within the tuning range as shown in Fig. 19(a). Fig. 19(b) shows the phase noise plot, at an output frequency of 227 GHz. The performance summary of the proposed VCO architecture and its

$$[Y_P] = \begin{bmatrix} \left(G_{\mathrm{PG}} + \dfrac{1}{L_G s} + \dfrac{C_C s}{L_C C_C s^2 + R_C C_C s + 1}\right) & \left(\dfrac{C_C s}{L_C C_C s^2 + R_C C_C s + 1}\right) \\ \left(\dfrac{C_C s}{L_C C_C s^2 + R_C C_C s + 1}\right) & \left(\dfrac{C_C s}{L_C C_C s^2 + R_C C_C s + 1} + G_{\mathrm{PD}} + \dfrac{1}{L_D s}\right) \end{bmatrix} \tag{14}$$

comparison to state-of-the-art CMOS signal sources operating between 200 and 300 GHz are presented in Table I. As a complete signal source, the proposed design achieves one of the highest η_p. A recent design in 65-nm CMOS achieves an even higher η_p of 4.6% [28], although by elevating the V_{DD} to 1.6 V.

VII. Conclusion

Impediments to enhance the output power and dc-to-RF power efficiency of VCOs operating near or above $f_{\max}$ of MOS transistors are investigated. The influence of the drain current waveform, transistor's large-signal output conductance, and the loss of the output power combining/matching network are studied. To improve the dc-to-RF power efficiency for a specific power consumption, the dc-to-RF current efficiency must be increased simultaneously with a decrease in output conductance. This is difficult to realize in harmonic oscillators because of a fundamental trade-off between power generation at the fundamental and at a higher harmonic. A VCO architecture based on frequency-multiplier is presented that ameliorates this tradeoff for efficient power generation. The use of a distinct class-C harmonic generator block and a power-efficient fundamental oscillator to drive it are proposed. Implemented in a 65-nm bulk CMOS process and operating at 219 to 232 GHz, the VCO attains a peak output power and dc-to-RF efficiency of 3 dBm and 3%, respectively. Future work will investigate the impact of second harmonics [28], [33] in further improving the dc-to-RF efficiency of multiplier-based sources.

Appendix

The half-circuit of the proposed oscillator at f_0 is shown in Fig. 20. The ideal 1:1 transformer models the cross-coupled feedback of the oscillator. The current flowing into the input matching network of the doubler is shown by I_m. I_1 and I_2 represents the fundamental current flowing into the gate and the drain, respectively, at the optimum A_g, A_d, and φ. It should be noted that I_1, I_2, and I_m can be obtained using simulations explained in Section IV. The passive network is represented with its Y-parameter $[Y_P]$

$$[Y_P]\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} -I_1 - I_m \\ -I_2 \end{bmatrix}. \tag{13}$$

It is straightforward to derive $[Y_P]$ as (14), shown at the top of this page, where $G_{\mathrm{PD}} = 1/R_{\mathrm{PD}}$, and $G_{\mathrm{PG}} = 1/R_{\mathrm{PG}}$ denote the loss in L_G and L_D, respectively. By assuming $V_2/V_1 = K_{\mathrm{opt}} e^{j\varphi_{\mathrm{opt}}}$, and solving (13) using (14), the desired passive network components are found.

Acknowledgment

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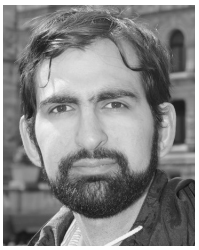

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