A 980μW 5.2dB-NF Current-Reused Direct-Conversion Bluetooth-Low-Energy Receiver in 40nm CMOS

Amir H. Masnadi Shirazi[1,2], Hossein Miri Lavasani[1], Mojtaba Sharifzadeh[1], Yashar Rajavi[1], Shahriar Mirabbasi[2], and Mazhareddin Taghivand[1]

[1]Qulacomm Inc., San Jose, California; [2]University of British Columbia, Vancouver, Canada

Abstract—This work presents a 980μW direct-conversion BLE receiver at a 1V supply, employing current-reuse and subthreshold techniques. The receiver has a measured noise figure of 5.2dB, integrated from 10kHz to 1MHz, that corresponds to a sensitivity of -95.8dBm. At a receiver gain of 47dB, an IIP3 of −19.7dBm has been measured. The LO integrated phase noise at 2.4GHz is 0.83° with LO spot phase noise of −119.9dBc/Hz at 3MHz frequency offset. The PLL is compacted inside the VCO inductor and has LC-VCO with a tuning range of 4.55GHz to 5.15GHz. Multiple μW-level feedback control loops are used in the design to make it robust over PVT variation. The prototype is implemented in a 40nm LP CMOS process occupying a silicon area of 0.7mm². To the best of our knowledge, the proposed receiver achieves the highest reported figure of merit among the BLE receivers published in the literature.

Index Terms— Low power Wireless, Subthreshold, Current-Reuse, Bluetooth Low Energy, CMOS, receiver

I. INTRODUCTION

Ultra-low-power wireless communication is one of the key enabling technologies for many smart networking applications including Internet of Things (IoT). Over the past decade, Bluetooth Low Energy® (BLE) has been one of the most popular standards for such low-power wireless systems [1]-[4]. To deliver a low power solution, most BLE transceivers trade off power consumption with performance. However, by incorporating innovative low-power circuit design techniques, it is possible to drastically reduce the power consumption in today's advanced radio architectures while delivering competitive performance. Current re-use and subthreshold designs in RF blocks are among the most promising techniques used in modern low power radios, most of which not only suffer from performance degradation over process, voltage, and temperature (PVT) but also they are sensitive to the choice of receiver architectures.

Receiver (RX) architectures such as discrete-time (DT) low-IF and continues-time (CT) sliding IF (SIF) have been used for BLE radios [2]-[5]. The low-IF and SIF topologies suffer from a problematic image that should be rejected by power-hungry multi-stage active filters and downconverters (local oscillators and mixers). This results in a high power consumption for receivers which target sensitivities better than -95dBm. There may also be a need to use high-Q off-chip (or on-chip) filters to further reject the image before the front-ends, as multiple local oscillator (LO) frequencies and associated spurs could desensitize the RX through reciprocal mixing. The RF filtering also increases the cost and degrades the noise figure (NF).
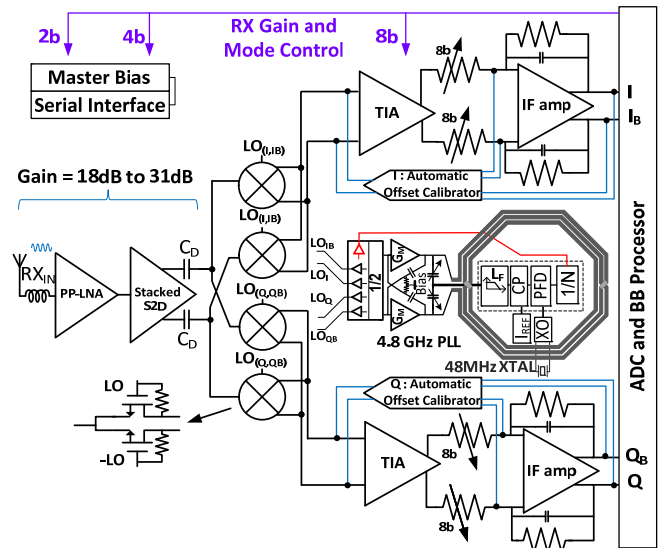

Fig. 1. Block diagram of the proposed ultra-low power direct conversion BLE receiver

This work presents a low power direct conversion receiver (DCR), employing current-reuse and subthreshold designs, with a simple double-frequency VCO that eliminates the intermediate down-conversion steps and the associated circuitry, while achieving sub-mW power consumption. Compared to other RX architectures, the DCR has minimal issues with reciprocal mixing of the LO harmonics and spurs. However, special attention has to be paid to DC-offset and I/Q mismatch issues, both of which call for a fully differential operation [6].

To alleviate these complexities with minimal power penalty, in this paper, a 980μW subthreshold current-reused fully-differential direct-conversion BLE receiver in 40nm CMOS is proposed in which multiple μW-level feedbacks are used to make the design robust over PVT (Fig. 1). The rest of this paper is organized as follows. Section II elaborates on the proposed low-power and high gain LNA. Section III presents the design, implementation, and measured performance of the compact PLL. Section IV discusses the implementation of the baseband amplifier and DC-offset cancellation block. Implementation details, receiver measurement results, and conclusions are provided in Section V and Section VI, respectively.
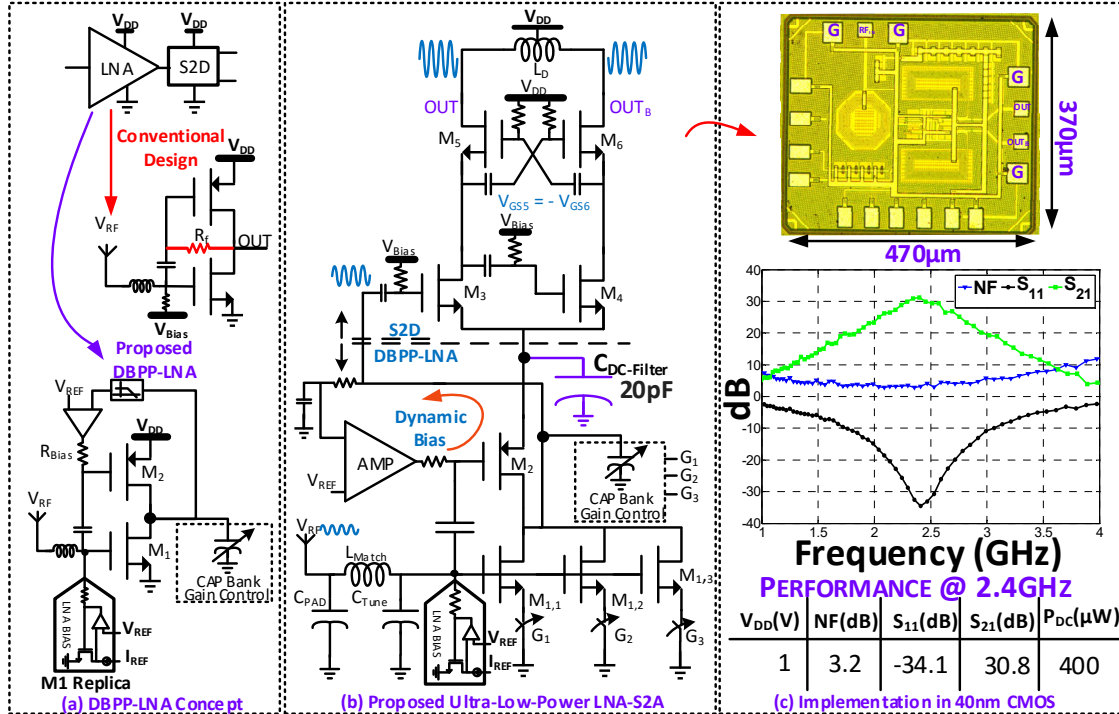
Fig. 2. (a) Block diagram, (b) schematic, and (c) measured standalone performance of the proposed ultra-low-power, PVT robust high gain LNA-S2D

II. PROPOSED PVT ROBUST LOW POWER LNA

The proposed differential LNA is shown in Fig. 2. The single-ended-to-differential (S2D) converter is stacked on top of the LNA to reduce the power consumption. The LNA uses a subthreshold current-reuse push-pull structure (PP-LNA) with a single-inductor input matching network. The effective transconductance of the LNA can be written as $g_{mp}+g_{mn}$ and hence, as compared to an NMOS-only design, it achieves similar gain with lower power. The push-pull also improves the linearity of the low noise amplifier [7]-[8].

The conventional biasing technique for PP-LNA uses a resistive feedback, namely R_F, to set the output DC voltage of the LNA to ~ VDD/2 (Fig. 2a). Although using R_F simplifies the design, in the stacked topology, the output DC voltage varies across PVT which significantly impacts the gain and input matching (S_{11}) of the subthreshold-biased LNA. The proposed dynamic-biased PP-LNA (DBPP-LNA), however, resolves the PVT variation issue by using a dynamically biased feedback loop, which forces the output DC level of the LNA to an adjustable and well-controlled voltage, V_{ref} (Fig. 2.a). To perform single-to-differential conversion while increasing the overall gain of the RF front-end, an active S2D converter consisting of two input common-source (CS) buffers followed by a Gm-boosted active balun is used (Fig. 2b). The CS-stages boost the LNA signal and provide a differential V_{GS} for M_5 and M_6 ($V_{GS5} = -V_{GS6}$) resulting in negligible amplitude and phase imbalance in the presence of device mismatch. The amplitude mismatch is negligible due to the high gain of the active balun. The L_D resonates out the capacitance at mixer input node near 2.4GHz allowing the current to flow through the mixer. In

addition, to save power, the current of the S2D converter is reused in the LNA by stacking the two stages on top of each other. A 20pF decoupling-cap (C_{DC}-filer) provides a high frequency AC-short for both the LNA supply and the S2D ground.. The stacked design provides a gain of over 30dB and a NF of less than 3.2dB while consuming 400μW from a 1V supply (Fig. 2c). To properly characterize the LNA-S2D, a separate test structure was designed (Fig. 2c) and measured using RF probes and a vector network analyzer (VNA).

III. PROPOSED LOW POWER AND COMPACT PLL

An integer-N PLL operating at twice the carrier frequency is used for downconversion. A CMOS 4.8GHz VCO with programmable PMOS gate-bias is implemented as shown in Fig. 3a. To minimize the VCO power consumption, $Q_{tank} \times L_{tank}$, that is the product of VCO inductance and its Q, is maximized. The VCO consumes less than 150μW. The VCO has a tuning range of 4.55 GHz to 5.15 GHz. The output frequency of the VCO is divided by two using a quadrature CML divider with resistive load (Fig. 3b). The VCO design was optimized to achieve low phase noise at the offset frequency of 3MHz to alleviate reciprocal mixing of the interferers in the adjacent channel. To reduce the silicon area, the PLL building blocks are physically placed inside a 3-turn VCO inductor, implemented in the copper ultra-thick metal (UTM), which reduces the Q by 6% according to EM simulations but results in over 8% of total area saving (Fig. 3c). The PLL, including the VCO, consumes 280μW and achieves an integrated phase noise (1kHz to 1MHz) of 0.83° (Fig. 3d) and a spot phase noise of -119.9 dBc/Hz at 3MHz offset. The LO, including the divide by two and the buffers driving the down-converting mixers, consume 230μW.
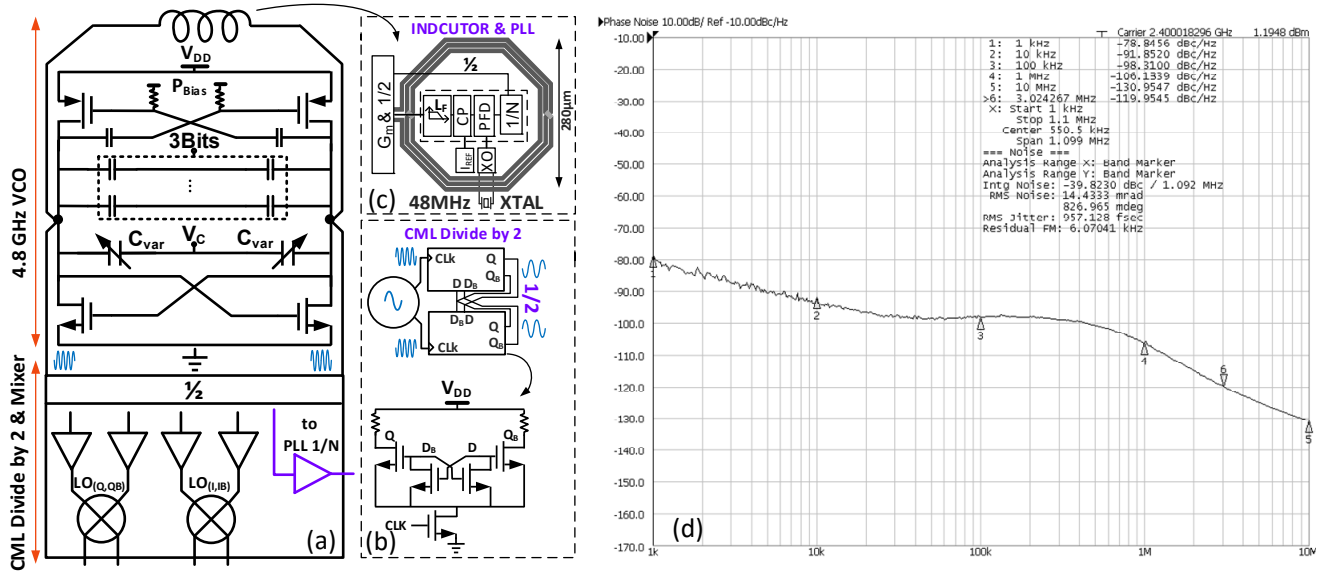
Fig. 3. Proposed frequency synthesis approach showing (a) VCO and (b) CML divider as well as the (c) block diagram and (d) measured phase noise of the PLL

IV. PROPOSED LOW-POWER BASEBAND AMPLIFIER

The down-converted current signal is absorbed by a two-stage programmable baseband amplifier (Fig. 4). To maximize the absorbption of the input current, a differential regulated-cascode (RGC) transimpedance amplifier (TIA) is employed as the input stage. It can be shown that by using an active load for the proposed TIA (namely M_3 in Fig. 4), the input impedance is independent of bias current, I_{tail}, and can be written as:

$$Z_{in-TIA} \approx 1/((r_{o1}||r_{o3}) \times g_{m1} \cdot g_{m5}) \; \alpha \; (\lambda_n + \lambda_p)\sqrt{\frac{L_1 L_5}{W_5 W_1}}$$

Where g_m, r_o, and λ are the transconductance, output impedance, and channel-length modulation of transistors.
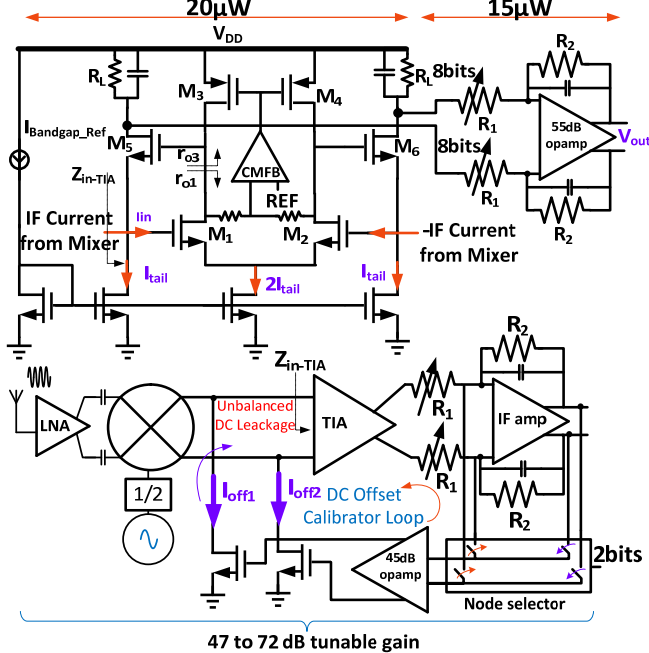

Fig. 4. Low-power baseband amplifier and automatic offset calibrator

Following the TIA, the second stage is a programmable differential voltage amplifier which employs a tunable shunt-shunt feedback with 12dB of tuning range . The overal baseband gain can be written as:

$$Gain \approx R_L R_2/R_1$$

A common-mode feedback loop is included within each differential stage. Input DC offset of the basedband amplifier is a potential concern for the system performance as the DC signal experiences a large gain before reaching the output. To address this issue, an analog DC offset cancellation feedback loop is used in which a sense amplifier balances the output DC levels by injecting a current into the input of the TIA (Fig. 4).

V. IMPLEMENTATION DETAILS AND MEASUREMENT RESULTS

The low power BLE receiver (including the compact all-in-inductor PLL) is fabricated in a 40nm LP CMOS process and occupies 0.7mm^2 (Fig. 5). A picture of the test PC board is also shown in Fig. 5.
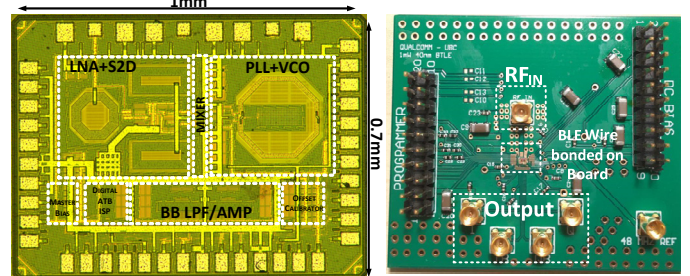

Fig. 5 Chip micrograph and test board of the proposed BLE receiver.

Fig. 6 shows the measured S_{11}, NF, and linearity performance of the receiver when consuming 980uA from 1V supply. At 980µW, the receiver achieves a NF of 5.2dB integrated from 10kHz to 1MHz (Fig. 6a) and a sensitivity of −95.8dBm. The LNA shows in-band $S_{11} < $ -15dB indicating very good matching to 50Ω (Fig. 6b). The gain can be changed from 47dB to 72dB by adjusting the gain of the LNA and baseband amplifier.
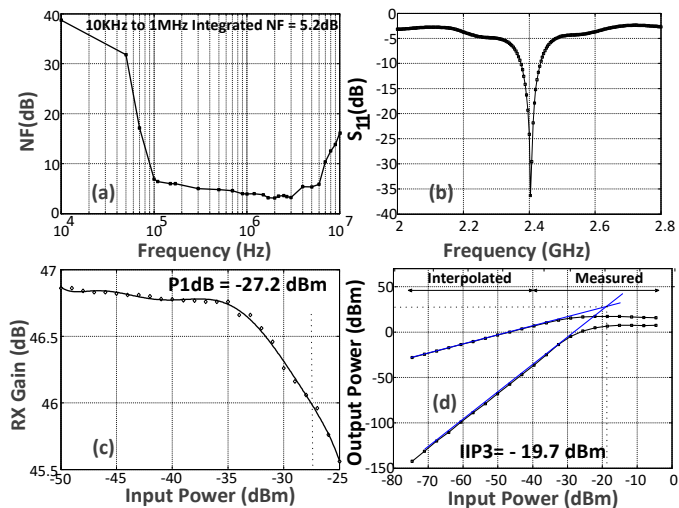
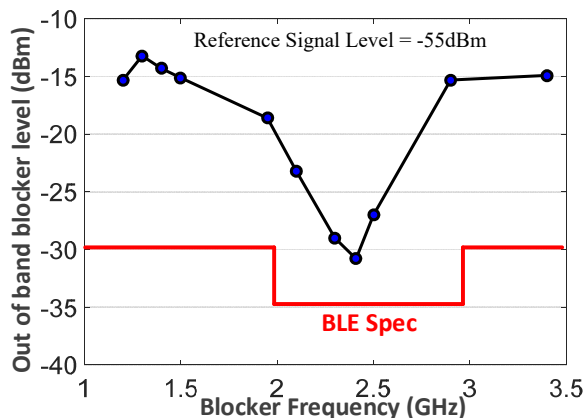Fig. 6. Measured NF, input S_{11}, P1dB, and IIP3 of the BLE receiver

Fig. 7. Blocking performance of proposed BLE receiver

At gain setting of 47dB, the system IIP3 and P1dB are −19.7dBm and -27.2dBm, respectively (Fig. 6c and 6d). The measured blocker performance of the receiver at gain setting of 47dB is shown in Fig. 7. The selectivity of the on-chip matching network of the LNA combined with narrowband nature of the LC tank load of the S2D help reduce the interference to an acceptable limit, meeting the BLE specification. The BLE receiver performance is compared with that of the state-of-the-art BLE radios in Table I. The integration of PLL loop-filter inside the VCO inductor has reduced the total chip area to 0.7mm². The receiver achieves a figure of merit [2] of -95.9dB which is an indication of better sensitivity and lower power consumption compared to published state-of-the-art designs. The design also offers lower NF with comparable linearity and smaller chip area than advanced BLE radios.

VI. CONCLUSION

A PVT-robust, ultra-low power, and compact direct conversion receiver is presented. It is shown that the proposed DBPP-LNA and stacked S2D can be implemented with sub-μW levels while providing high gain at first stage, which further supresses the NF of consecutive stages. To reduce VCO-LNA leakage a compact PLL-in-inductor at twice the input carrier frequency is implemented. The baseband utilises a TIA

followed by VGA and uses active DC-offset calibrator, essential for direct conversion receivers. A proof-of-concept prototype 1-Mbps GFSK BLE with configurable gain from 47 to 72dB, is designed and fabricated in a 40nm CMOS LP technology. The receiver achieves a RX sensitivity of -95.8dBm at 980μW with FoM of -95.9, which to the best knowledge of the authors, is the highest reported FoM among the BLE receivers published in literature.

TABLE 1. PERFORMANCE SUMMARY OF STATE-OF-THE BLE RECEIVERS

Reference	[1]	[2]	[3]	[4]	This Work
Data Rate & Modulation	1-Mbps GFSK	1-Mbps GFSK	1-Mbps GFSK	1-Mbps GFSK	1-Mbps GFSK
Architecture	DC	TD-SIF	TD-SIF	DT-Low IF	DC
Integrated NF (dB)	N/A	6.5	N/A	6.5	5.2
RX Gain (dB)	NA	NA	N/A	48	47-72
RX Sensitivity (dBm)	-94.5	-94.5	-94	-95	-95.8
RX IIP3 (dBm)	N/A	N/A	N/A	-19 @48dB Gain	-19.7 @47dB Gain
Integrated PN(°)	N/A	N/A	N/A	0.87	0.83
PN @ 3MHz	N/A	N/A	N/A	N/A	-119.9
Supply Voltage (V)	0.9-3.3	1.1	1	1	1
P_{DC}(mW)	11.2	6.3	3.3	2.75	0.98
Chip Area(mm²)	2.9	1.1	1.3	1.84	0.7 (RX)
*FoM	-84	-86.5	-88.8	-90.1	-95.9
Technology	55nm CMOS	40nm CMOS	40nm CMOS	28nm CMOS	40nm CMOS

* RX Figure of Merit (FoM) $= RX_{Sensitivity} + 10\log(\frac{Power}{1mW})$

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