A Novel Active Decoupling Capacitor Design in 90nm CMOS

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***Abstract*—On-chip decoupling capacitors (decaps) are generally used to reduce power supply noise. Passive decap designs are reaching their limits in 90nm CMOS technology due to higher operating frequency, lower supply voltage, increased concerns on electrostatic discharge (ESD) reliability and thin-oxide gate leakage. In this paper, a novel active decap design is proposed to provide better noise reduction than the passive decaps. The active decap is analyzed for ESD reliability and process/temperature variation adaptability. It is implemented in a 1.0V-core 90nm process with a total area of 0.168mm^2 and standby power of 3.0mW.**

I. Introduction

As technology scales, it becomes more challenging to maintain the quality of power supply due to increased clock frequency and decreased supply voltage. Decoupling capacitors (decaps) are typically used to reduce IR drop and Ldi/dt effects, and hence keep the power supply within a certain percentage (e.g., 10%) of the nominal supply voltage [1]. Prior to the 90nm node, a passive decap layout using NMOS transistors in a CMOS process [2] was sufficient. At 90nm, the oxide thickness has been reduced to 2nm or less. Therefore, decaps have been redesigned into a cross-coupled form [3] to protect the device from potential electrostatic discharge (ESD) induced oxide breakdown. However, the cross-coupled design and its modifications [4] significantly reduce the transient response of the decap. In addition, gate tunneling leakage current increases considerably due to the thin oxide. Overdesign of decaps, as used in the past, must be avoided to minimize static power. Therefore, it is necessary to design an ESD-safe active decap that provides better performance in a small area with low leakage.

Two *active decap* circuits using switched capacitances have been proposed to regulate the supply voltages [5]-[7]. By increasing charge delivery capability, the two designs in [5] and [7] are effective in reducing supply noise, but there are also limitations associated with each. It was observed that [5] performs well but dissipates excessive power, whereas [7] saves power but experiences excessively long delays. They both address the issue of LC resonance, which is less significant in 90nm or beyond mainly due to increased on-chip decoupling capacitance. Based on a similar concept of switched decaps, this paper proposes a novel active decap design that has lower power than [5] and better response than [7]. For 90nm CMOS designs, the active decap must be ESD safe and adaptable for larger process and temperature variations.

The remainder of the paper is organized as follows. In Section II, the design concept of switched decaps is briefly discussed. The active decap architecture is then analyzed in Section III. The comparator design, a key component of the active decap, is proposed in Section IV. Section V shows the active decap layout and simulation. Conclusions are provided in Section VI.

II. Switched Decoupling Capacitors

The fundamental concept of the active decap is to switch a pair of passive decaps either in parallel or in series, as illustrated in Fig. 1 [5]-[7]. Initially, the decaps are in the parallel configuration. When switched in series, the power-grid voltages are boosted up. When switched back in parallel, the voltages are reduced.

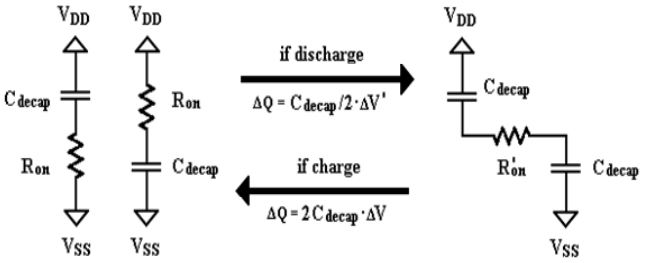

Figure 1. Concept of switched decaps [5]-[7].

In the standby state, two passive decaps are placed in parallel, resulting in an equivalent capacitance of $2C_{decap}$. The total charge accumulated at the capacitors is $\Delta Q = 2C_{decap}\Delta V$, where ΔV is the voltage difference on the power grid, $V_{DD} - V_{SS}$. When the power grid discharges (e.g., current flows into a switching logic gate), the voltage difference ΔV between V_{DD} and V_{SS} will reduce as well. A sensing circuit magnifies this voltage difference and switches the two parallel capacitors into a series connection. When the capacitors switch, the charge ΔQ cannot vary instantaneously, and thus remains at its initial value for a short while. The equivalent capacitance, however, shrinks to $C_{decap}/2$ by stacking the two capacitors in series. As a result, the new $\Delta V'$ turns out to be $4\Delta V$. In other words, the power grid

voltages V_{DD} and V_{SS} are boosted up (ideally) by a factor of four. In practice, this can never be achieved mainly because the power mesh and the decap circuitry non-idealities limit the excessive voltage variations on-chip. Similarly, in the charging stage, when the power grid voltages are charged up and are above the nominal supply voltage, the two capacitors are switched from series to parallel, which returns the voltages roughly back to their original values.

The switches in the circuit are implemented using MOS transistors. One possible configuration is depicted in Fig. 2 [5]-[7]. The two NMOS and two PMOS transistors operate as switches. When the capacitors are in parallel, both Mn1 and Mp1 are on while both Mn2 and Mp2 are off (or in subthreshold). When the capacitors are in series, both Mn1 and Mp1 are off while both Mn2 and Mp2 are on.

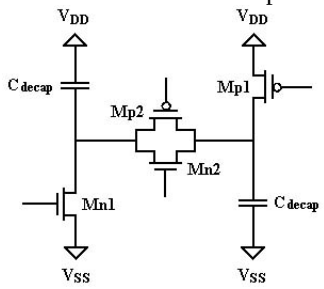

Figure 2. MOS implemented switched decaps [5]-[7].

The "on" resistances, R_{on}, of the switch transistors are the device channel resistances. When in parallel, the R_{on}'s of Mn1 and Mp1 are connected to the decaps. When in series, the new R_{on} is the parallel combination of the "on" resistances of Mn2 and Mp2, as previously shown in Fig. 1. Considering ESD reliability, LC resonance and ohmic losses in decap performance, the "on" resistances should be kept in the range of 10 ohms by increasing the transistor widths. Specifically, the transistor widths are designed in the range of 500um in 90nm. However, with such large switches, the drivers generating the switching signals need to be strong enough, resulting in a large sensing and switching circuitry that consumes a considerable amount of power and area.

III. Active Decap Architecture

The proposed active decap contains four main blocks: a reference voltage generator, a pair of high-pass filters, twin comparators, and switched decaps, as illustrated in Fig. 3. In the same figure, a user logic circuit block is placed close to the active decap and is the main cause of power grid noise.

The switching circuit in the active decap is realized using twin comparators. The differential inputs of each comparator decide the standby voltage level at the outputs of the comparators. In the standby mode, Comparator 1 has an output at V_{DD}, whereas Comparator 2 is set at V_{SS}. When the power grid discharges, V_{DD} will drop and V_{SS} will rise. The instantaneous voltage variations are passed through the high-pass filters and force the comparator inputs to switch. Thus, the comparators will reverse their output values, switching the decaps from parallel to series. When the power grid charges up, the comparator inputs are switched back, as are the outputs of the comparators. The two comparators use identical designs to better adapt to process and temperature variations in 90nm.

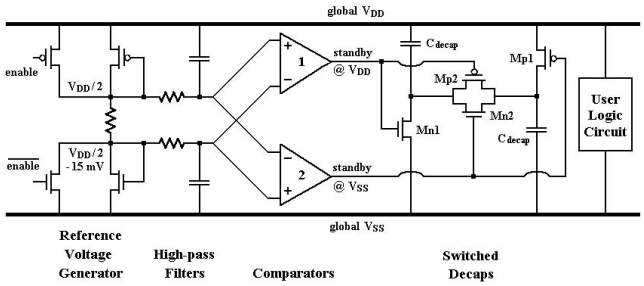

Figure 3. Active decap architecture.

The *RC*-based high-pass filters of Fig. 3 are required to provide a cut-off frequency above 10MHz, filtering out low-frequency voltage fluctuations to save power. The reference voltages are generated by a simple voltage divider and are set to roughly $V_{DD}/2$. Inserting a resistor between the two nodes further separates the reference voltages by 15mV. The comparators are intended to switch once the voltage (V_{DD}-V_{SS}) discharges by 30-40mV, which can be considered as the sensitivity of the active decap. Depending on the comparator design, the absolute input levels of $V_{DD}/2$ are somewhat flexible due to the differential nature of the inputs. An *enable* signal is also provided for testing purposes.

IV. Comparator Design

When the decaps are in parallel, the subthreshold leakage from the switches consumes considerable power, due to the large sizes of the transistors. To reduce leakage current, the outputs of the comparators should be as close as possible to either V_{DD} or V_{SS}. Hence, a comparator with a full swing output is desired, although a slightly larger switching current may be needed. The input variation is less than 100mV and the output is full swing, indicating the need for high gain in the switching region. With all the above considerations, a two-stage op-amp based comparator was designed, as shown in Fig. 4.

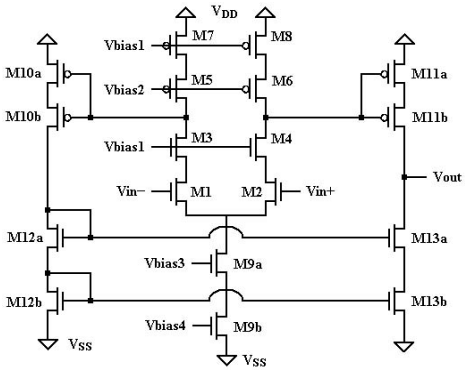

Figure 4. Comparator design.

The two-stage design satisfies the need for high gain and full swing. The first stage is cascoded to provide high gain,

while the second stage uses an active current mirror to generate a full swing. Generally, a cascode structure sees limited use in deep submicron analog designs due to reduced voltage headroom and low supply voltage. However, it is suitable in this case because the design is used for large signal amplifications. Assuming symmetry, the small-signal open-loop gain for the first stage, $|A_{v1}|$, is approximately:

$$|A_{v1}| \approx g_{m1}(g_{m3}r_{o1}r_{o3} // g_{m5}r_{o5}r_{o7}) \quad (1)$$

where g_m is the transconductance and r_o is the output resistance of the transistor.

The second stage converts the differential signals into a signal-ended output. The full swing is achieved through the use of a cascode current mirror, which increases the output resistance. The second stage is an output buffer, where the desired slew rate can be determined by adjusting the transistor sizes. If needed, offset cancellation techniques may be applied, although not implemented here. The large-signal dc characteristics of the comparator are illustrated in Fig. 5. The switching threshold is ±10mV, and the peak dc gain is above 50. When power grid noise is at 100mV (V_{DD}-V_{SS}), the switching delay for a full swing is approximately 2.2ns.

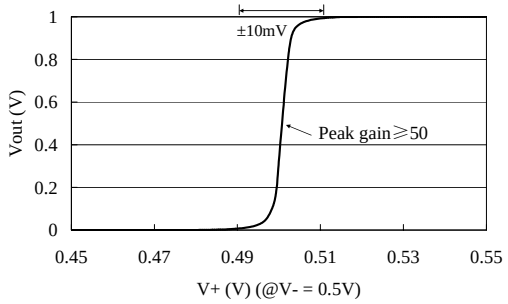

Figure 5. DC transfer curve of the comparator.

This two-stage comparator design has a number of advantages: high gain, full output swing, low noise, low offset, high tolerance on process and temperature variations, and lower power consumption than [5]. The nature of the large-signal comparator and its slew rate improves the stability of the design. In addition, the cascode design ensures ESD reliability. As a drawback, the speed for such a comparator design is relatively low, although better than [7]. This makes it most suitable for frequencies associated with ASIC designs.

V. Layout and Simulation

The layout of the active decap was implemented in a TSMC 90nm 1.0V-core process and is shown in Fig. 6. The switching circuitry is located in the center, whereas the two passive switched decaps are on each side. The decap on the left is made of N-type MOSFETs, while the one on the right is P-type. The decaps are formed using thin-oxide transistors to improve area efficiency. The thin-oxide decaps have a certain amount of gate tunneling leakage current. Thick-oxide decaps can be used instead to reduce leakage, if necessary. Here, the use of thin-oxide decaps provides roughly a 1.0nF capacitance in the standby mode. The decap channel lengths are selected to provide sufficient transient response for a targeting operating frequency, according to [8]. The active decap layout uses Metal1 only, similar to the cell libraries, for the purpose of being integrated into the digital CAD flow at a later point. The Metal1-only configuration also eliminates the concerns on possible routing congestion. The interconnect widths are adjusted to satisfy the requirement of electromigration. A summary of the post-layout parameters is highlighted in Table I.

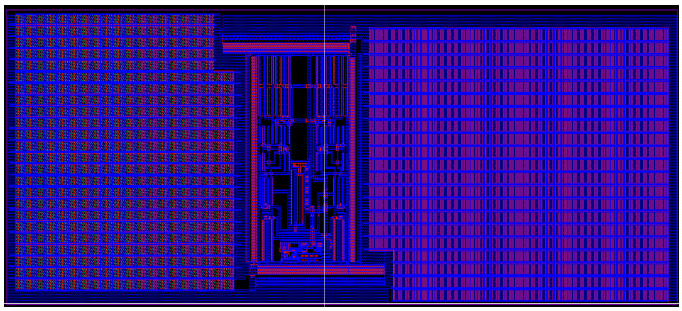

Figure 6. Active decap layout.

TABLE I. Summary of Post-Layout Parameters

Process	1.0V, 90nm CMOS
Total area	0.168mm^2
Switching circuitry area	0.031mm^2
Standby power (TT, 1V, 75°C)	3.0mW*
Passive decoupling capacitance	~1nF

*including thin-oxide decap gate leakage of 1.1mW.

Compared to passive decaps, active decaps provide better performance but at a cost of higher static power. Hence, active decaps should be only placed at locations where the power grid noise is excessive and there is empty space. After the severe IR-drop locations (often referred to as "hot spots") are identified, active decaps should be placed in these areas only. For other regions, passive decaps, including thick-oxide or cross-coupled decaps, may be used to control power [4]. By combining passive decaps and active decaps, designers are given greater design flexibility, and a better tradeoff of power, area, and performance may be achieved. Knowing the size of one active decap, the placement of active decaps may require other logic blocks to be shifted to accommodate them. Thus, it is recommended that the active decap placement is performed in the early stage of the design flow to avoid excessive routing/placement/timing iterations near the end of the physical design process.

Time-domain analysis with accurate *RLC* models is desired when estimating performance. As illustrated in Fig. 7, the simulation uses extracted *RLC* values from a wire-bond test chip in the same 90nm process. Package inductances are included. There are *n* pairs of V_{DD}/V_{SS} bond wires and pads in parallel. The worst-case power mesh resistance is used. The user logic circuit is represented by a current source, whose waveforms are obtained from the

current demand profiles of the test chip. The current demand profiles are obtained from RedHawk™ Apache™ in a vectorless mode.

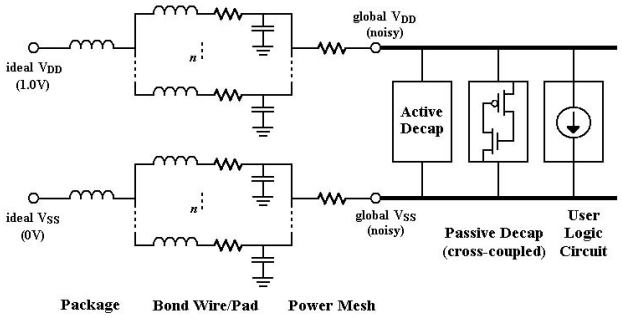

Figure 7. Time-domain simulation.

In the simulation, it is assumed that the total decap area including active decaps is fixed. It is also assumed that 50% of the total area is occupied by active decaps and the rest 50% is passive cross-coupled decaps. Note that this combination is used to illustrate the concept of active decaps only, and may not be optimal. The optimal placement of active decaps that balances power consumption and power grid noise reduction will be investigated as future research. For performance, Fig. 8 illustrates a comparison between passive+active decaps and passive-only decaps, for a fixed area. The combination of active and passive decaps provides better capability of holding the power grid voltages and charging them up. Also shown in Table II, the average voltage drop at V_{DD} that controls the path delay is much lower for the combined active and passive decaps, even though the worst-case voltage drop is about the same. However, the reduced power grid noise is at a cost of increased power consumption.

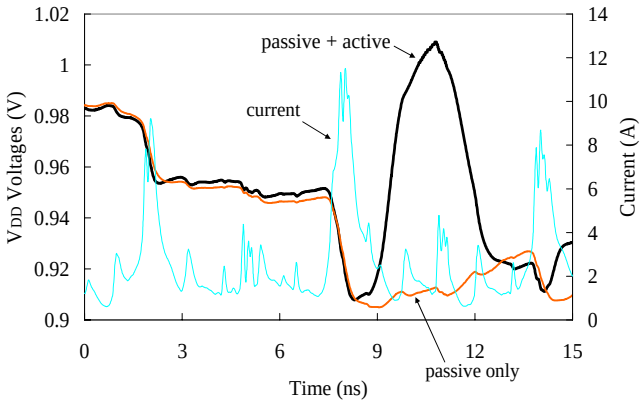

Figure 8. Voltage comparison at the V_{DD} rail.

TABLE II. VOLTAGE DROP COMPARISON

	Worst-case drop	**Average drop**
Passive and active	92mV	**47mV**
Passive only	95mV	**63mV**

In addition, the active decap satisfies the ESD requirement of a design. Using a human body model and following the standard MIL-STD-883x method 3015.7 [9], ESD simulations were also carried out. With one power clamp added as the primary protection element [4], all nodes are within the safe voltage range, meaning that the active decap is ESD reliable in 90nm.

VI. CONCLUSIONS

This paper proposes improvements to the design of an active decoupling capacitor for power grid noise reduction. Based on the concept of switched decaps, the active decap amplifies the charge storage capacity of the passive decap while monitoring the power rail activity to provide dynamic control of the switching response. The ESD-reliable active decap design makes proper tradeoffs between performance, power consumption and area. The key components of the active decap are the twin comparators, which were designed to adapt for large process/temperature variations and to provide high gain and full output swing at relatively low power. Simulations in 90nm indicate that the combination of active and passive decaps provides a smaller average voltage drop for less power grid noise and shorter path delay when operated at ASIC frequencies.

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