Timothy Rogers
Curriculum Vitae

Research Interests

Hardware architectures and software systems that enable **programmer productivity** in a **performant and energy efficient manner**. I am particularly interested in investigating techniques that **break layers** of the general purpose computing stack.

Education

Ph.D.in Computer Engineering 2010-2015
University of British Columbia, Vancouver, BC, Canada

→ Thesis: *Locality and Scheduling in the Massively Multithreaded Era*

Honors B.Eng with distinction in Electrical Engineering 2001-2005
McGill University, Montreal, QC, Canada

→ Honors Thesis: *Optical Reception for Gigabit Ethernet*

Selected Honors and Awards

Communications of the ACM (CACM) Research Highlight 2014

→ One of 12 papers per year in all computing-research conferences selected by CACM as an outstanding research article.

NVIDIA Graduate Fellowship Winner 2013

→ $25k. One of 11 winners from top students worldwide. (https://research.nvidia.com/content/nvidia-graduate-fellowship-results-2013)

NVIDIA Graduate Fellowship Finalist 2014

→ One of 5 finalists selected from top students worldwide. (https://research.nvidia.com/content/2014-grad-fellows)

IEEE Micro Top Picks from Computer Architecture 2012

→ One of 11 papers selected from all computer architecture conferences.

NSERC Alexander Graham Bell Canada Graduate Scholarship 2013

→ 105k over 3 years. Major Canadian scholarship awarded to top Ph.D. students.

MICRO-45 Best Paper Runner-up 2012

MICRO-45 Best Lightning Presentation Runner-up 2012

→ *https://www.youtube.com/watch?v=92OszNy6L0M#t=13m17s*

204-2710 Acadia Road, Vancouver BC
timrogers@gmail.com | https://www.ece.ubc.ca/~tgrogers/

University of British Columbia Four Year Fellowship 2013

→ 72k over 4 years plus tuition.

UBC Faculty of Applied Science Graduate Award 2013

→ 9k. Awarded by UBC applied science department to outstanding graduate students

McGill Student Athlete Academic Honor Roll 2001-2004

Undergraduate scholarships totaling 20k 2001-2005

Governor General of Canada's Academic Medal 2001

→ Highest academic average in secondary school

Publications

Conference and Journal Papers* (see appendix)

T.G. Rogers, D.R. Johnson, M. O'Connor, S.W. Keckler, *Variable Warp Sizing.* To appear in proceedings of the 42nd IEEE/ACM International Symposium on Computer Architecture (ISCA-2015), Portland, OR **ISCA 2015**

→ Acceptance Rate: 19.0%

T.G. Rogers, M. O'Connor, T.M. Aamodt,*Learning Your Limit: Managing Massively Multithreaded Caches Through Scheduling.* Research Highlight in Communications of the ACM (CACM), vol. 57, no. 12, December 2014 **CACM 2014**

→ Invited publication

T.G. Rogers, M. O'Connor, T.M. Aamodt, *Cache-Conscious Thread Scheduling for Massively Multithreaded Processors.* IEEE Micro, Special Issue: Micro's Top Picks from 2012 Computer Architecture Conferences **IEEE MICRO TOP PICKS 2013**

T.G. Rogers, M. O'Connor, T.M. Aamodt, *Divergence-Aware Warp Scheduling.* In proceedings of the 46th IEEE/ACM International Symposium on Microarchitecture (MICRO-46), Davis, CA **MICRO 2013**

→ Acceptance Rate: 16.3%

T.G. Rogers, M. O'Connor, T.M. Aamodt, *Cache-Conscious Wavefront Scheduling.* In proceedings of the 45th IEEE/ACM International Symposium on Microarchitecture (MICRO-45), Vancouver, BC **MICRO 2012**

→ **Best Paper Runner-Up**

→ **Selected for CACM Research Highlight**

→ **Selected for IEEE MICRO Top Picks**

→ Acceptance Rate: 17.5%

T. H. Hetherington, **T. G. Rogers**, L. Hsu, M. O'Connor, T. M. Aamodt, *Characterizing and Evaluating a Key-Value Store Application on Heterogeneous CPU-GPU Systems.* In Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), New Brunswick, NJ **ISPASS 2012**

→ Acceptance Rate: 30.8%

Posters/Workshops

T.G. Rogers, M. O'Connor, T.M. Aamodt, *Divergence-Aware Warp Scheduling.* Poster at NVIDIA GPU Technology Conference 2014, San Jose, CA **GTC-2014**

Tech Reports/Manuals

GPGPU-Sim Manual Contributor 2014

→ http://gpgpu-sim.org/manual/index.php5/GPGPU-Sim_3.x_Manual

Patents

Rogers, Timothy G.; Beckmann; Bradford M.; O'Connor; James M., *CREATING SIMD EFFICIENT CODE BY TRANSFERRING REGISTER STATE THROUGH COMMON MEMORY*, United States Patent Application #20140149710, May 29, 2014. Assignee: Advanced Micro Devices Inc. 2014

Rogers, Timothy G.; Beckmann; Bradford M.; O'Connor; James M., HIGH LEVEL SOFTWARE EXECUTION MASK OVERRIDE , United States Patent Application #20140181467, June 26, 2014. Assignee: Advanced Micro Devices Inc. 2014

Rogers, Timothy G.; Beckmann; Bradford M.; O'Connor; James M., DATA PROCESSOR AND METHOD OF LANE REALIGNMENT, United States Patent Application #20150100758, April 9, 2015. Assignee: Advanced Micro Devices Inc. 2015

First inventor on one other currently undisclosed US patents with NVIDIA Corporation 2014

Professional Experience

Assistant Professor, Purdue University, West Lafayette, IN 2016

- → Electrical and Computer Engineering Department beginning January 2016

Architecture Research Intern, NVIDIA, Austin, TX Spring 2014

- → GPU processor core research activities improving the energy efficiency of emerging and existing programs.
- → Performed studies in the production C++ hardware simulator used by product teams to define next generation architectures.
- → Work resulted in ISCA-2015 paper.
- → Filed one US patent application.

Architecture Research Intern, AMD, Bellevue, WA Spring 2012

- → Heterogeneous GPU/CPU research activities improving processor efficiency on emerging workloads.
- → Filed three US patent applications.

Software Engineer, Electronic Arts, Burnaby, BC, Canada 2006-2010

- → Programmed runtime C/C++ game code, C/C# tools and Action Script front end menu code
- → Shipped 6 titles across four hardware platforms (Xbox 360, Sony PS3, Nintendo Wii, Sony PSP) with various roles including rendering engineer, lead audio programmer, gameplay programmer, front end programmer and core systems engineer.

Software Developer, Apparent Networks, Vancouver, BC 2005-2006

- → Programmed Java code for the Company's network analysis tool. Worked on elements of the frontend GUI, web interface and server-side code.
- → Lead developer for the internal license management software and the core product's installer.

Software Developer Intern, Got Marketing, Montreal, QC Summer 2004

- → Proposed, designed and implemented the front-end of an internal customer tracking tool.

Teaching Experience

Sessional Instruction

UBC EECE 476: Computer Architecture Spring 2015

- → Sole instructor for a class of 83 students
- → Taught fundamentals of computer architecture using various active learning techniques.

Teaching Assistant

UBC EECE 259: Introduction to Microcomputers Fall 2014

- → Tutoring and marking for 300 Students
- → Assisted course development by scoping out assignments, creating and validating the lab infrastructure and providing feedback on course direction
- → Administered lab where students wired basic logic components gates, wrote VHDL for a microcomputer capable of running a subset of the ARM ISA, performed assembly and high-level C programming.

UBC EECE 381: Computer Systems Design Studio Spring 2013

- → Tutoring and marking for 30 Students
- → Administered a hands-on lab where students programmed NIOS processors on Altera DE2 boards, interfacing them with handheld android devices.

UBC EECE 476: Computer Architecture Fall 2012

- → Tutoring and marking for 75 Students
- → Assisted course development by creating assignments.
- → Occasionally lectured in place of the professor.

UBC EECE 353: Digital Systems Design Fall 2011

- → Tutoring and marking for 150 Students
- → Administered lab session where students coded VHDL.
- → Occasionally lectured in place of the professor.

Professional Workshops

Instruction Skills Workshop (http://iswnetwork.ca/) 2014

- → 3-day interactive workshop on developing/practicing active learning techniques.

Tutoring

Private Tutor, Montreal, QC 2002-2005

→ Tutored undergraduate students in math and CS.

Selected Talks

Writing Efficient Code, Without All the Work, Three Minute Thesis competition presentation. 2015

→ ***2nd Place in UBC Applied Science Faculty.***

→ ***People's Choice Award***

Learning Your Limit: Managing Massively Multithreaded Caches Through Scheduling, online presentation accompanying CACM Research Highlight 2014

→ ***Link Pending***

Locality-Conscious GPU Architectures, San Jose, CA. NVIDIA graduate fellowship winner presentation. 2014

Divergence-Aware Warp Scheduling, Davis, CA. MICRO-46 full paper presentation, poster presentation and lightning presentations 2013

Why Professors are like GPUs: How to Manage Massively Multithreaded Caches Through Scheduling, Vancouver, BC Presentation of Communications of the ACM (CACM) Research Highlight material to UBC ECE faculty 2013

Cache-Conscious Wavefront Scheduling, Vancouver, BC, Canada. MICRO-45 full paper presentation, poster presentation and lightning presentations 2012

→ **Best Lightning Presentation Runner-Up**

→ *https://www.youtube.com/watch?v=92OszNy6L0M#t=13m17s*

Research Community Service

ISPASS 2016 Program Committee Member	**ISPASS-2016**
1st Annual Warp Scheduling Championship (held in conjunction with MICRO-2015) co-organizer	**WSC-2015**
Invited reviewer for Computer Architecture Letters (CAL)	**CAL-2015** **CAL-2014**
External reviewer for International Symposium on Microarchitecture (MICRO)	**MICRO-2013**
Invited reviewer for IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)	**ISPASS-2013**
Invited reviewer for International Inter-national Journal of High Performance Computing (IJHPC)	**IJHPC-2012**
External reviewer for International Conference on Parallel Architectures and Compilation Techniques (PACT)	**PACT-2012**

Extra-Curricular Activities

McGill Varsity Field Lacrosse Team
High School and Club Baseball Team Captain
High School, Club and Recreational Goaltender

Volunteer Work

Minor Hockey Goaltending Coach
Minor Baseball Assistant Coach

Memberships

Golden Key International Honor Society
ACM

Appendix

*(**Credited to Prof. Tor Aamodt's CV**): "For those not familiar with the field of computer architecture, publication in top international conferences is the *preferred* means of disseminating research results in this area. Papers in proceedings of top conferences, often with acceptance rates below 20%, are more important than journals. See Chapter 4 in the 1994 National Academy of Sciences report, Academic Careers for Experimental Computer Scientists and Engineers http://books.nap.edu/html/acesc/ and the 1999 Best Practices Memo: Evaluating Computer Scientists and Engineers For Promotion and Tenure http://www.cra.org/uploads/documents/resources/bpmemos/tenure_review.pdf. The top computer architecture conferences are ISCA, MICRO, HPCA, ASPLOS and PACT. The review process at these conferences is very rigorous: Program committee (PC) members are internationally recognized experts in the field. Each paper typically receives four or more double-blind reviews (3 or more from PC members) providing detailed feedback. Authors submit responses to questions raised by reviewers prior to the PC meeting, which is attended in-person by PC members. Accepted papers are revised to reflect reviewer feedback before publication. High quality papers deemed to be on the borderline of accept/reject often undergo an additional round of review by a PC member after revision and before final acceptance for publication (a process known as "shepherding"). Added together, the five conferences above publish only 150 to 200 papers per year. Due to their impact, these conferences are very well attended. Given their importance, papers published in the proceedings of these conferences are read and cited by active researchers in the area even if those researchers did not attend the conference."