ROBERTO ROSALES

www.linkedin.com/in/2RobertoRosales Email: 2Roberto.Rosales@gmail.com

RESEARCH AND TEST ENGINEER

Resourceful and dynamic Electrical Engineer with strong background and wide-ranging expertise in analog/RF IC design. Skilled at all stages of IC design, and final verification, with a proven record of effective problem solving and commitment to goals. Consistently excels and is widely valued for contributions to work environment and the ability to lead change. Experienced in:

- R&D team leadership
- Design and setup of R&D test facilities
- Management of R&D test laboratories
- Design and modelling of CMOS and bipolar analog ICs
- Use and support of CAD tools
- IC characterization techniques: on-wafer probing, RF, mmWave, parametric, etc.
- Use, selection, and maintenance of test instruments.
- Design and implementation of test structures and characterization circuits.

TECHNICAL SKILLS

Design

- DC/ LF/ RF/ Microwave
- Discrete circuits from conception to product.
- CMOS Integrated circuits, p35, p18, 90nm, 65nm, 45nm.
- Bipolar Integrated circuits, NT25 High Speed Bipolar
- Printed Circuit Boards and test structures
- R&D test facilities

CAD and Computing

- Cadence Analog Artist
- SpectreRF, HSpice, Spice
- Agilent ADS
- Calibre LVS, extraction
- Matlab
- Labview
- IC-CAP
- Protel/Altium, Multisim, OrCad
- C++, HTML, PASCAL, BASIC
- Unix (Solaris), Linux (Debian), MS Windows

Instrumentation

- Real time and sampling Oscilloscopes.
- Spectrum, Network, and Parameter analyzers
- Signal/RF/Microwave sources
- On wafer probe stations, and probes
- Wire bonders
- BER testers
- RF/Microwave components
- Instrumentation control

PROFESSIONAL EXPERIENCE

THE UNIVERSITY OF BRITISH COLUMBIA, 2001 - present
Department of Electrical and Computer Engineering, Vancouver, BC.

SoC Test Lab Manager **2003 - present**
Managed the UBC System-on-Chip test facilities and provided technical support for the design and test of research ICs. Participated directly in joint research projects. Managed the operational logistics for the SoC Research group, and for 18 months simultaneously performed as interim CAD Manager.

- Managed laboratory resources including: $2M worth of equipment and tools, equipment grants, space, training materials, support websites, and junior staff.

- Provided technical support towards the design and testing of over 52 ICs, as well as numerous dissertations and research publications.
- Designed, advised on, debugged, or conceived circuits implemented in various technologies from TSMC, STM, IBM, and DALSA, and covering applications in RF communications, sensors, implants, on-chip measurements, device characterization, embedded SoC testing, and power line communications.
- Conceived, designed, advised on, and built test fixtures, test accessories, and instrumentation setups for: on-wafer probing of loose dice ICs, die-on board testing of loose dice, and on-board testing of packaged ICs.
- Developed and maintained training materials, and support web-pages.
- Participated in joint research with faculty and graduate students, in the areas of device characterization, on-chip jitter measurement, and most recently vehicular power-line communications.
- Performed as acting System-on-Chip CAD Manager for a total period of 18 months, providing support for Cadence, Mentor, Synopsis, Agilent, Altera, and Xilinx tools. Led system migration from Solaris based machines to Debian, resulting in a dramatic improvement of the group's design activities. Upgraded or repaired a pool of over 90 computers and performed annual license renewals.
- Managed group logistics for the 67 members of the SoC Research group, including access, enforcement of regulations, operational finances, maintenance of physical facilities and computer resources, groups web pages, mailing lists, etc.

Technical Consultant **2001 - 2003**

Assisted the Dept of Electrical and Computer Engineering in the design, setup and launch of the System-on-Chip Test lab, managed the initial operations of the test lab, and provided technical support for graduate IC design and for various undergraduate projects.

- Provided guidelines for the construction and equipment of the UBC SoC Test Laboratory, and contributed to the design of the student office areas.
- Created procedures and regulations for the use of the test facilities.
- Executed $700K of purchase grants for additional equipment of the SoC Test Lab.
- Provided technical support towards the design and test of over 13 integrated circuits and various other discrete projects.
- Conceived and supervised graduate self-directed study courses in the area of instrumentation, as well as supervised undergraduate co-op students and research related under-graduate course projects.

EDUCATION

PhD., Electrical Engineering, University of British Columbia.
MASc., Electrical Engineering, University of British Columbia.
BSEE., Universidad Simon Bolivar, Caracas – Venezuela.

LANGUAGES

Native or bilingual proficiency: **English**, **Spanish**, Full professional proficiency: **French**.

Full addendum of technical publications can be found at:
www.ece.ubc.ca/~robertor/Home.htm