

# Critique of High-Frequency Performance of Carbon Nanotube FETs

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Abstract—The emerging body of literature on the high-frequency performance of carbon nanotube field-effect transistors (CNFETs) is critically reviewed. The focus is on the figure-of-merit  $f_T$ , the common-source, short-circuit current gain. The intentions are: to direct attention to the most relevant measured data; to compare this data with record values for other transistors, and with predicted results for CNFETs; to explain the large spread in predicted data; to offer a prognosis for high-frequency CNFETs.

## I. Introduction

The high conductivity and band-gap tunability are just two of the many properties that render carbon nanotubes of interest for electronic devices. Field-effect transistors have been made from these molecules, and their DC performance and switching capabilities have been reviewed [1]. The potentially high transconductance of CNFETs, and the low capacitance that might possibly be associated with a nanoscale device, make CNFETs also of interest for small-signal, high-frequency applications. Experimental data for Schottky-barrier-contacted (SB-) CNFETs in various high-frequency circuit configurations is beginning to accumulate, and theoretical predictions of  $f_T$  abound. It is timely to review all of this work: to pick out the experimental data that relates directly to the high-frequency capability of CNFETs, and to compare this to the simulation data that predicts performance limits, and also identifies limitations to performance due to intrinsic and extrinsic factors. There is also a controversial prediction for doped-contact (C-) CNFETs that needs to be assessed. All of these issues regarding high-frequency performance are addressed in this review. An opinion on the likelihood of CNFETs being used in high-frequency applications is also offered.

## II. Experimental

The low current-drive and high input/output impedance of single CNFETs make it difficult to perform direct measurements of high-frequency electrical properties using instrumentation based on a reference impedance of  $50\Omega$ . Attempts to avoid these difficulties by creative measurement techniques, or by employment of CNFETs as microwave detectors or resonators, have been reviewed [2], [3]. Additional work falling in these categories has appeared very recently [4], [5].

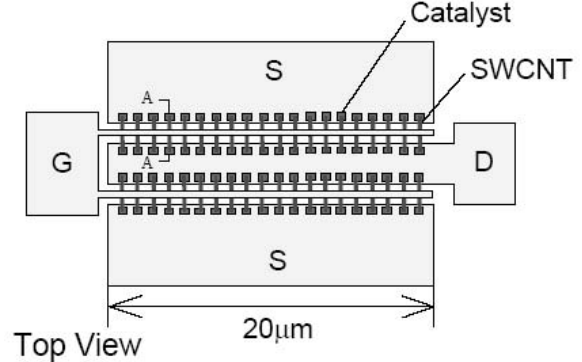


Fig. 1. Top view of CNFET employing many single-wall carbon nanotubes, as used in high-frequency measurements [8].

In order to make a direct measurement of a recognized high-frequency figure-of-merit, such as  $f_T$ , it has been realized that CNFETs assembled from multiple nanotubes must be employed [6], [7], [8], (see Fig. 1). Such measurements are in their infancy, and problems of non-parallel nanotubes, the presence of some metallic nanotubes, and excessive gate overlap capacitance need to be addressed. However, progress is being made, and the highest  $f_T$  recorded thus far, after de-embedding, is 10.3 GHz [8].

The experimental data is shown in Fig. 2: it can be seen that it does exhibit a dependence on gate length  $L_G$ , which is indicative of the success of the de-embedding procedures in removing the effect of the pad parasitics. The figure also shows the gate-length dependence of  $f_T$  as predicted in the “ideal propagation-delay limit”, i.e., when the signal delay is determined solely by the propagation of electrons through the gated portion of the nanotube [9], or, in other words, when the capacitance associated with the change in charge in the gated, intrinsic portion of the tube  $C_{Gi}$ , dominates both the parasitic capacitance and the capacitance due to changes in charge in regions of the CNFET external to the gated-portion  $C_{Ge}$ . Clearly, such an ideal situation cannot be attained in practice, but the comparison emphasizes that effort should be put into making measurements on structures using shorter nanotubes. Certainly, as Fig. 2 also shows, shorter channel lengths or basewidths have been employed to

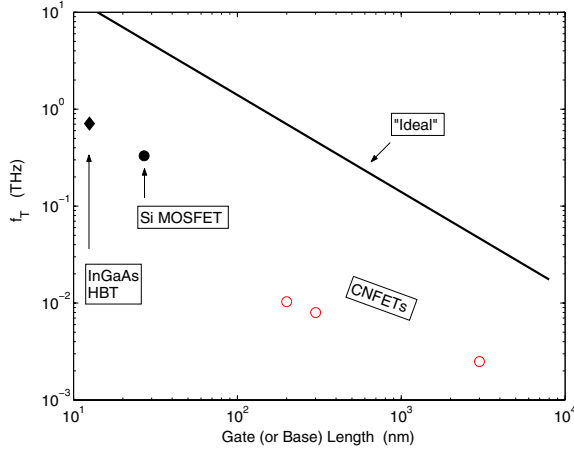


Fig. 2. Experimental data from high-frequency transistors. CNFETs - open circles [6], [7], [8]. SiCMOS - filled circle [10]. HBT - filled diamond [11]. The “ideal” curve is from Eq. (2).

obtain record  $f_T$  values for other transistors: Si MOSFETs (330 GHz [10]) and InP/InGaAs HBTs (710 GHz [11]).

### III. Theoretical

Detailed theoretical analyses involve the self-consistent solution of the equations of Schrödinger and Poisson, usually under the quasi-static approximation [12]. Methods involving either an effective-mass wave equation, or a Hamiltonian based on atomistic considerations, have been employed, and, under suitably low-bias conditions, should give similar results [13], provided the simulation space is properly bounded [14].

The extrapolated  $f_T$  is given by

$$2\pi f_T = \frac{\partial I_D}{\partial Q_G} \equiv \frac{g_m}{C_{Gi} + C_{Ge}}, \quad (1)$$

where  $\partial I_D$  and  $\partial Q_G$  are changes in drain current and gate charge, respectively, due to a change in gate-source voltage, for example;  $g_m$  is the transconductance, and the internal and external contributions to the total gate capacitance  $C_{GG}$  have been described earlier. The “ideal propagation-delay limit” (IPL), referred to above, proposes

$$2\pi f_{T,\text{ideal}} = \frac{v_{\text{Fermi}}}{L_G}, \quad (2)$$

where  $v_{\text{Fermi}}$  is the maximum, band-structure-limited velocity that can be attained in some, long, zig-zag nanotubes: its value depends on the choice of the overlap parameter used in the tight-binding approximation to get the band structure. Here we use a value such that  $f_{T,\text{ideal}}$  in THz is given by  $140/L_G$ , with  $L_G$  in nm. This number represents a fundamental limit, and is preferred to  $80/L_G$  [15], which is a phenomenological limit.

#### A. Schottky-barrier CNFETs

Both coaxial and planar Schottky-barrier CNFETs have been studied, e.g., see Fig. 3 [16] and Fig. 4 [18]. Results

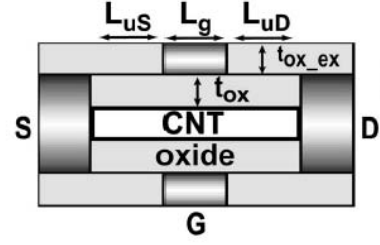


Fig. 3. Coaxial Schottky-barrier CNFET with wrap-around gate [16].

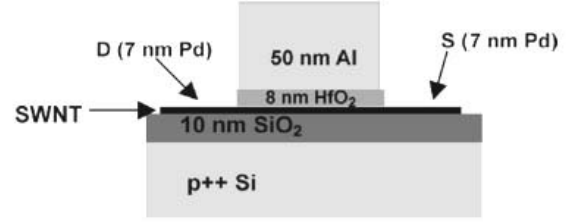


Fig. 4. Planar, top-gated Schottky-barrier CNFET [18].

are shown in Fig. 5 for the effect of  $C_{Ge}$  on  $f_T$  for both of these structures.

For the  $L_G = 2$  nm case the effect is large because of the small gate-source underlap  $L_{uS}$  (14 nm). In the  $L_G = 5$  nm case, increasing the separation of source and drain electrodes to 24 nm mitigates the effect. The results shown are for contact radii varying from that of the nanotube itself, to that of the nanotube plus oxide and gate thicknesses [17]. For the planar,  $L_G = 50$  nm case, the degradation of  $f_T$  is due to changing the contact from that of a needle of radius equal to that of the nanotube, to that of a metallic strip of width  $8 \mu\text{m}$ . The latter was

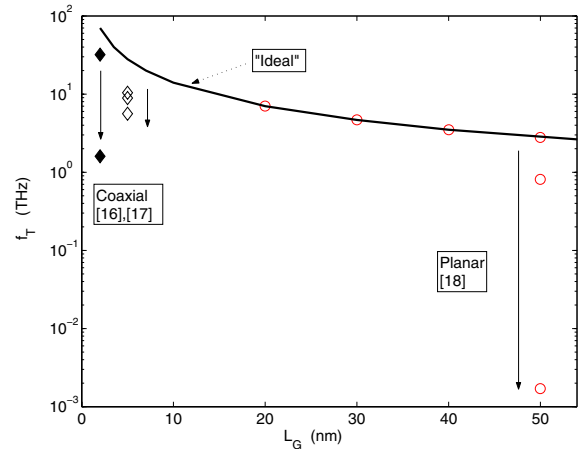


Fig. 5. Effect of the external gate capacitance on  $f_T$ . Solid arrows indicate increasing  $C_{Ge}$ .

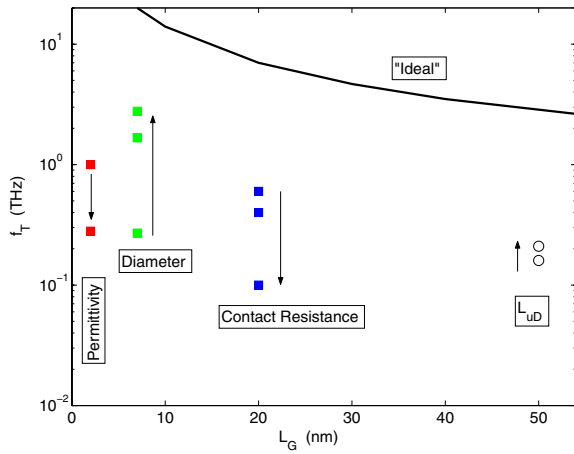


Fig. 6. Effect of various parameters on  $f_T$ : oxide permittivity and nanotube diameter [20]; contact resistance [22]; gate-drain underlap [24]. Arrows indicate increasing parameter.

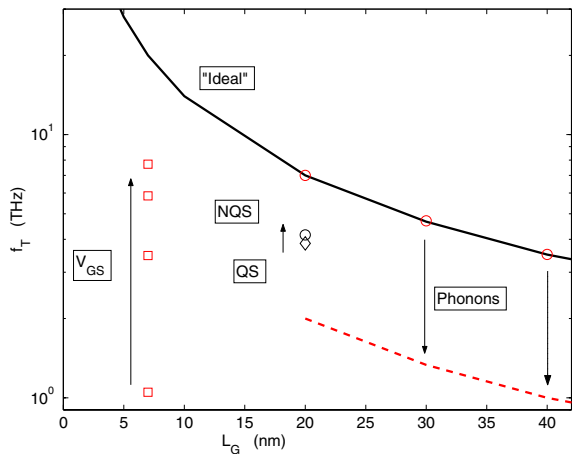


Fig. 7. Effect on  $f_T$  of: gate bias [25]; non-quasi-static response [26]; phonon scattering [27]. Arrows indicate increasing parameter.

the actual electrode structure of a high-performance DC device [19], and emphasizes the need to develop finer contact arrangements for HF devices. The data points falling on the “ideal” curve are interesting because they are presumably from a full, self-consistent solution [18], not merely from Eq. (2). It is difficult to imagine how all the carriers could be propagating at  $v_{\text{Fermi}}$ , because some of them would populate states near the bottom of the band, for which a lower velocity applies.

The effects on  $f_T$  of varying oxide permittivity, nanotube diameter, gate-drain underlap, and contact resistance are shown in Fig. 6. Increasing  $\epsilon_{ox}$  from 3.9 to 25 decreases  $f_T$ , principally via an increase of the gate capacitance [20]. For Schottky-barrier contacts representing palladium, the barrier height for hole injection decreases as the nanotube diameter increases [21]. This enhances  $g_m$ , leading to the improved performance shown in Fig. 6 on changing the diameter from 0.8 nm through 1.3 to

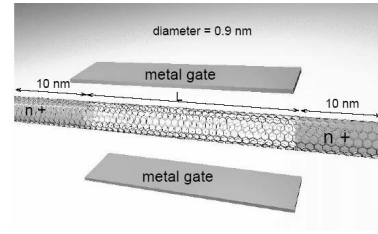


Fig. 8. Doped-contact CNFET with double-gate [28].

1.7 nm [20]. Increasing the separation of the gate and drain electrodes reduces one contribution to  $C_{Ge}$ , so  $f_T$  is improved, as Fig. 6 shows for the case of  $L_{uD}$  being increased from 5 to 25 nm [24]. The figure also shows the effect of considering the actual resistance of the source and drain contacts. Such resistances can be expected to be high when employing nanoscale needle contacts. The results shown are for  $R_{\text{contact}}$  increasing from zero through 10 k $\Omega$  to 100 k $\Omega$  [22]. Similar degradations also apply to  $f_{\text{max}}$  [23]. The gate-source voltage  $V_{GS}$  has a significant effect on  $f_T$ , mainly via  $g_m$ , which, for the case of electron injection, increases as the barrier at the source is either lowered or thinned. The results shown in Fig. 7 indicate the improvement for a particular CNFET on increasing  $V_{GS}$  from 0.4 to 0.7 V, with  $V_{DS}$  held at 0.7 V [25]. This improvement may be mitigated at other combinations of  $V_{GS}$  and  $V_{DS}$ , due to the bias dependence of  $C_{Gi}$  [12].

Fig. 7 also addresses two issues that have not been considered hitherto: scattering and non-quasi-static response. More data is needed on the latter, but, presently, a non-quasi-static analysis does not appear to be necessary, at least at the frequencies around 1 THz that have been examined thus far [26]. On the other hand, phonon scattering could be important, at least in tubes of length greater than about 10-20 nm, which is the mean-free-path for optical phonons [27]. Phonon scattering leads to a build-up of charge in the channel, i.e., to an increase in  $C_{Gi}$  [27].

## B. Doped-contact CNFETs

Doped-contact CNFETs, such as shown in Fig. 8, have not been studied as extensively as SB-CNFETs, although they appear promising for HF applications: a higher  $g_m$  can be expected, due to the reduced quantum-mechanical reflection of electrons at the injecting doped/intrinsic interface within the nanotube. The present data may be sparse, but some of it is certainly provocative: Fig. 9 shows that some of the predictions for  $f_T$  are above the IPL. Of course, the relevant delay time  $\tau_r$  for a region of length  $r$  is the signal delay time  $\int_r \partial Q_G(z)/\partial I_D dz$ , which is not necessarily equal to the propagation delay time [25]. For example, in quasi-neutral regions, such as the doped contacts far away from the gated region,  $\tau_r = 0$  (actually, the signal delay in such cases is the dielectric relaxation time). Also, in regions supporting an electric

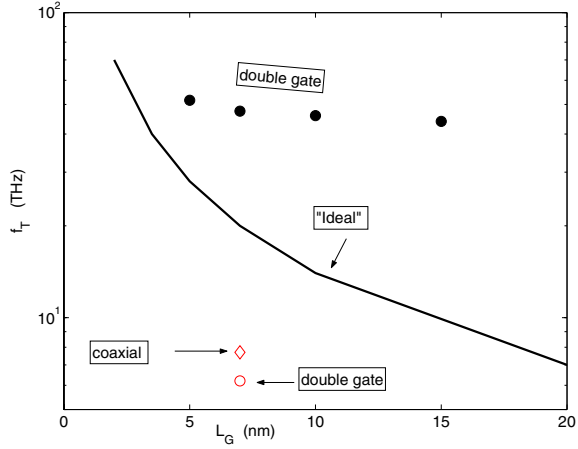


Fig. 9. Effect on  $f_T$  of gate length for doped-contact CNFETs. Double-gate devices: filled circles [28], open circle [29]. Coaxial device - diamond [25].

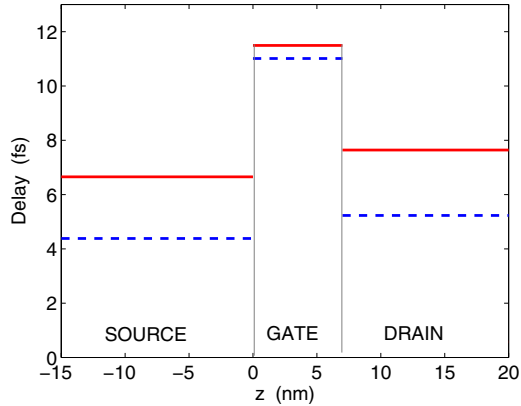


Fig. 10. Regional signal delays for the open-symbol data of Fig. 9: coaxial device - dashed line, double-gate device - solid line [29].

field, such as in the base-collector depletion region of an HBT, field-adjustment leads to image charges, not all of which contribute to the input charge  $\partial Q_{\text{base}}$ ; so the signal delay becomes less than the propagation delay. In the C-CNFET, in the space-charge regions of interest, fields are present, but all image charges are complemented by changes in  $\partial Q_G$ , so it is difficult to see how the propagation delay can be bettered.

The regional signal delays are shown in Fig. 10 for the devices that yielded the open-symbol data in Fig. 9. As expected, the largest delay is in the gated portion of the nanotube, but note the very significant contribution (about 50%) from the adjacent space-charge regions, i.e.,  $C_{Ge} \approx 0.5C_{Gi}$  in these examples. Note also that the delay in any one of the three regions depicted in Fig. 10 is greater than the total delay of 3.4 fs implied by the results of Ref. [28] for  $L_G = 7$  nm. Thus, this extraordinary result is presently unconfirmed and inexplicable.

### C. Prognosis for high-frequency CNFETs

Inevitably, when considering the performance of a new field-effect transistor, comparisons will be made with Si MOSFETs. This review has suggested that the signal velocity in the non-neutral regions of FETs is unlikely to exceed the band-limited propagation velocity,  $v_{\text{band}}$ . Thus, a relevant question is: how does  $v_{\text{band}}$  for carbon nanotubes compare with that in nanoscale Si structures? Guo et al. have suggested that  $v_{\text{band}}$  for an ultra-thin body Si MOSFET is about 50% of that in a CNFET [18]. Wang et al. compute average carrier velocities for Si nanowires that are about 4 times lower than typical values of  $v_{\text{Fermi}}$  for CNFETs [30]. Thus, as regards the gated portion of the FET, it seems reasonable to state that a CNFET cannot reduce the signal delay by more than a factor of 2-4 below that of a nanoscale Si FET.

These comparisons are for ballistic transport, and it may be argued that attainment of ballistic transport is more likely in a CNFET than in a Si MOSFET, primarily because of the relatively long mean-free-path for phonons in carbon nanotubes, but also because of their more one-dimensional form. However, it seems unreasonable to ignore the effect of surface scattering, which greatly affects the mobility in present Si MOSFETs. The nature of the oxide/semiconductor interface is different in the two devices, of course, but some penetration of the electron wavefunctions into the oxide of a CNFET is to be expected. There is presently no information on this, to the author's knowledge.

The signal delay in the space-charge regions proximal to the gated region of the nanotube, in other words the external capacitance  $C_{Ge}$ , contributes significantly to  $f_T$ , and a point to mention here is that simulated results are usually for the case of zero gate-thickness. Thickening the gate so that the gate resistance does not prohibit attainment of a high  $f_{\text{max}}$ , will lead to a widening of the space-charge regions in the source and drain of doped nanotubes, or to an increase in the interelectrode capacitance of SB-CNFETs. In each case,  $f_T$  will be reduced below the values discussed in this paper.

The strong effect of source and drain resistance on  $f_T$ , as illustrated in Fig. 6, is another issue of practical importance. Add this to the gate-resistance issue, and to the need to arrange CNFETs in parallel to improve the current drive, and one wonders whether the small material superiority of  $v_{\text{band}}$  and the geometrical superiorities of a wrap-around gate and a one-dimensional structure, will be enough to combat the matchless technological superiority of silicon FET processing. Perhaps the high-frequency performance of CNFETs can be exploited in biological situations, with which carbon should be more compatible than silicon?

### IV. Conclusions

From this review of the high-frequency performance of CNFETs it can be concluded that:

- experimental  $f_T$  values should improve by employing multiple, parallel nanotubes of shorter length than used hitherto;
- theoretically, the effects on  $f_T$  of nanotube diameter, oxide permittivity, gate-source and gate-drain underlap, electrode diameter, and phonon scattering are well understood;
- the effects of surface scattering and gate thickness need to be addressed;
- non-quasi-static effects may not be very important;
- the concensus of simulations to date implies that the signal delay time is not less than the propagation time. This suggests that the band-structure-determined velocity is a key factor in assessing the high-frequency prospects for a FET material. The slight advantage that a carbon nanotube has over silicon in this regard may not be sufficient to offset the technological superiority of Si FETs when it comes to processing practical devices.

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