CSTC Manuscript Number: **297**

Switching-speed calculations for Schottky-barrier carbon nanotube FETs

D.L. John and D.L. Pulfrey*

Department of Electrical and Computer Engineering,

University of British Columbia, Vancouver, BC V6T 1Z4, Canada

(Dated: January 8, 2006)

Abstract

The switching times and ON/OFF-current ratios are computed for Schottky-barrier carbon nanotube field-effect transistors with different tube diameters and insulator thicknesses. It is indicated that it may be difficult to obtain a device exhibiting both high speed and low leakage current. A small-diameter nanotube with a thin insulator may offer the best compromise. It is also demonstrated that inter-electrode capacitances can be large, thereby calling into question the usefulness of the intrinsic switching time as a figure-of-merit for transistors intended for digital-logic applications. The extrinsic switching time is a more appropriate metric, and it is shown here that considerable optimization of the carbon nanotube field-effect transistor will be required to achieve figures better than for modern Si CMOS transistors over a reasonable range of ON/OFF-current ratio.

I. INTRODUCTION

If the carbon nanotube field-effect transistor (CNFET) is to prove useful for digital applications, then it is a *sine qua non* that the device should have a short switching time τ, and a high ratio of ON-current to OFF-current $I_{\rm ON}/I_{\rm OFF}$. A way of computing τ from DC data, and relating it to $I_{\rm ON}/I_{\rm OFF}$, thereby providing a useful metric for devices with non-optimized threshold voltage,[1] has recently been proposed,[2] and used to predict sub-picosecond switching times for CNFETs out to $I_{\rm ON}/I_{\rm OFF} \approx 10^4$ in Ref. 3, or $\approx 10^2$ in Ref. 1. The method, in essence, estimates the time taken for a constant gate capacitance C_G of a single CNFET (the load), charged to a voltage V_{DD}, to be discharged through another CNFET (the driver) at a constant current $I_{\rm ON}$, where the latter is evaluated for the driver transistor at drain- and gate-source voltages, V_{DS} and V_{GS}, respectively, equal in magnitude to V_{DD}, thus:

$$\tau = \frac{C_G V_{DD}}{I_{\rm ON}}. \tag{1}$$

The method has merit because: (a) all parameters can be computed from a DC simulation performed at a single V_{DS}; (b) the discrepancies involved in using constant values for the discharge current and the gate capacitance tend to compensate each other.

In this paper we show the approximations involved in arriving at Eq. (1), and then use it to produce new results concerning the effect on τ of: (a) the nanotube diameter; (b) the extrinsic gate-source and gate-drain capacitances. We take into account the latest data on barrier heights,[4] and apply it to a planar structure based on a recent experimental Schottky-barrier (SB) CNFET with very high DC performance.[5] As the nanotube diameter reduces, and some reduction below that of the roughly 1.7 nm used in Ref. 5 is probably necessary for a digital device in order to obtain a respectable $I_{\rm ON}/I_{\rm OFF}$ ratio,[6] then the barrier height increases. Here, we show that this has a very significant effect on τ. Similarly, we show that the inclusion of the gate inter-electrode capacitances, thereby changing τ from a measure of the intrinsic switching speed to one of the extrinsic switching speed, has a pronounced effect.

II. THE MODEL

Consider Fig. 1 in which two identical FETs are arranged as a driver (transistor A) and as a load (transistor B). The load is discharged by a current i, given by

$$i(V_{GS}^A, V_{DS}^A) = \frac{\mathrm{d}Q_G^B(V_{GS}^B, V_{DS}^B)}{\mathrm{d}t},$$

where $V_{GS}^A = V_{DS}^B = -V_{DD}$, where V_{DD} is the positive supply voltage given by the difference between the OFF and ON gate voltages on the load, namely:

$$V_{DD} = V_{GS,\mathrm{OFF}}^B - V_{GS,\mathrm{ON}}^B.$$

The discharge current $i = -I_D^A$ will vary as the load discharges, but the practice is to evaluate i at its highest value, namely:

$$i = -I_D^A(-V_{DD}, V_{GS,\mathrm{ON}}^B) \equiv -I_{\mathrm{ON}}^A.$$

Expressing the change in nanotube charge in terms of a capacitance, we define

$$\frac{\partial Q_{\mathrm{CN}}^B}{\partial V_{GS}^B} = -C_G^B(V_{GS}^B, -V_{DD}),$$

where Q_{CN} is the charge on the carbon nanotube (CN) channel which is equal and opposite to that on the gate if inter-electrode capacitances are neglected. As Fig. 2 shows, C_G is not constant during the discharge period. The practice, however, is to evaluate it at its highest value, shown by the slope of the dashed line, namely:

$$C_G^B = C_G^B(V_{GS,\mathrm{ON}}^B, -V_{DD}) \equiv C_{G,\mathrm{ON}}^B.$$

This overestimate of C_G compensates somewhat for the overestimation of i in the resulting expression for the switching speed:

$$\tau = \frac{C_{G,\mathrm{ON}}^B V_{DD}}{|I_{\mathrm{ON}}^A|}. \tag{2}$$

The ratio $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ is evaluated by sliding a window of width V_{DD} along a plot of I_D *vs.* V_{GS}, as described previously.[3]

To evaluate $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, and the parameters appearing in Eq. (2), we perform simulations in which the equations of Schrödinger and Poisson are solved self-consistently[7] for the planar geometry SB-CNFET depicted in Fig. 3, where we assume that the azimuthal potential

variation on the surface of the CN is sufficiently small as to allow us to use the axial potential in our Schrödinger solution. The validity of this approximation will be the subject of a future work. Note that the gate electrode is a rectangular block above the nanotube, and the source, CN, and drain are all cylinders. The exact shape of the source and drain contacts is not as critical as the shape of the gate electrode, since the band bending near the contacts will be largely determined by the size of the contacts, and not their shape, when the nanotube is fixed in the centre of the contact. As a result, the source and drain geometry is chosen more for convenience than for its experimental feasibility.

III. RESULTS AND DISCUSSION

Results are presented here for the structure shown in Fig. 3, which, in the baseline case, has many properties similar to that of a recent, high-DC-performance experimental device,[5] namely: the nanotube has a diameter $2R_t = 1.7\,\mathrm{nm}$ (taken to correspond to a tube of chirality (22,0)), the insulator has a thickness $T_{\mathrm{ins}} = 8\,\mathrm{nm}$ and a relative permittivity of 16, as appropriate for hafnia, the end contacts are Pd, and the underlap of the gate and end-contacts is $L_{sg} = L_{dg} = 4\,\mathrm{nm}$. Other parameters for the baseline device are: gate length, thickness and breadth of 20, 5, and 10 nm, respectively; cylindrical end-contacts of radius $R_c = 6\,\mathrm{nm}$ and length $L_c = 1\,\mathrm{nm}$. The work function of the nanotube is $4.7\,\mathrm{eV}$,[8] and the work function of the gate is adjusted to give reasonable I_{ON} in the simulation range of $-1 < V_{GS}^{B} < -0.5\,\mathrm{V}$. The barrier height for the Pd/nanotube end-contacts is taken from very recent data,[4] and has a value of $-0.04\,\mathrm{eV}$ for holes in this case. Unless otherwise stated, simulations are performed at $V_{DS} = -0.5\,\mathrm{V}$, and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ is evaluated at $V_{DD} = 0.5\,\mathrm{V}$. The choice of this value is arbitrary,[1] and is used here as it may be realistic for far-future, low-voltage logic applications.

Fig. 4 shows the very poor $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of the baseline device. This arises from the low bandgap of the nanotube, *i.e.*, $\approx 0.5\,\mathrm{eV}$ for a (22,0) tube, which ensures that the Schottky barrier heights for electrons and holes are sufficiently similar that ambipolar conduction occurs before a low I_{OFF} can be attained.[1] To improve on this situation, a nanotube with a higher bandgap is called for.[3] Fig. 4 also shows the result for a (10,0) tube, for which the bandgap is $\approx 1\,\mathrm{eV}$. $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ is improved to $\approx 10^4$, albeit at the expense of a reduction in I_{ON} due to the higher barrier height for holes, *i.e.*, $+0.3\,\mathrm{eV}$ in this case.[4] One way to mitigate the

$I_{\rm ON}$ reduction would be to thin the tunneling barrier at the source by more tightly coupling, electrostatically, the gate to the nanotube. This can be achieved by reducing $T_{\rm ins}$, and the solid line in Fig. 4 shows the beneficial effect of having $T_{\rm ins} = 2\,{\rm nm}$ when using the (10,0) nanotube.

The intrinsic switching times for the three devices considered thus far are shown in Fig. 5. The high ON current in the (22,0) case yields a short τ, but the high OFF current limits $I_{\rm ON}/I_{\rm OFF}$ to low values. For the (10,0), thick-insulator case, the low drain current is responsible for the poor τ, and the increase in current brought about by thinning the gate insulator translates into an improvement in τ. In all three cases, although it is not apparent in the (10,0), thick-insulator case until longer values of τ than are shown in Fig. 5, $I_{\rm ON}/I_{\rm OFF}$ starts to decrease after reaching its maximum value. This corresponds to $V_{GS,{\rm OFF}}$ passing through, in a positive direction for the p-type devices considered here, the point at which $|I_D|$ is a minimum.[1] Additionally, the (10,0), thin-insulator case shows an increase in τ at the low end of its $I_{\rm ON}/I_{\rm OFF}$ range, which corresponds to operation at high, negative values of V_{GS}. To examine this phenomenon, consider Fig. 6, which shows the gate-bias dependence of the charge in the nanotube, from which the intrinsic capacitance is computed (see Fig. 2). It is clear that there is a pronounced increase in C_G as the negative gate bias reaches high values, and this is responsible for the increase in τ. The rise in charge comes about because the thinning of the potential barrier at the drain, due to the use of a thinner insulator, allows holes to tunnel into the nanotube at high, negative gate bias. The valence-band profiles for the two (10,0) cases, displayed in Fig. 7, show that this does not happen with a thicker insulator. This restriction of the operating range for the aggressively scaled device was not apparent in earlier work,[3] where it was assumed that a zero-height Schottky barrier could be obtained with a small-diameter nanotube.

The intrinsic switching time is a helpful metric for guiding initial device design[1] but, in practice, particularly in devices such as nanotube FETs where the electrodes are inevitably close together, an extrinsic τ, which accounts for the contribution of the inter-electrode capacitances to C_G, is more useful. In this case, we may apply Gauss' Law in order to compute the charge on the gate directly. This is facilitated through our use of the finite element method for the electrostatics problem, which provides direct information regarding

both the potential and the electric field. If we recall that

$$\oint_{\text{surf}} \mathbf{D} \cdot \mathrm{d}\mathbf{a} = Q_{f\text{enc}},$$

where d**a** is a differential area element multiplied by the unit outward normal vector, and we integrate the electric displacement, **D**, over a Gaussian surface that encloses the appropriate electrode, we may straightforwardly compute the charge enclosed, $Q_{f\text{enc}}$, inside that surface, and hence, we have the charge on that electrode. For the total extrinsic gate capacitance, we compute the total charge on the gate, while the intrinsic gate capacitance assumes that the charge on the gate is equal and opposite to that on the nanotube. The charge on the nanotube is known from the self-consistent solution procedure.

The results of doing this for our three devices are shown in Fig. 8. Even though we have used modest dimensions for the source and drain metalization, which would probably result in excessive series resistance, the contributions of the gate-source and gate-drain capacitances to C_G are huge, and lead to much larger switching times than predicted for the intrinsic cases. Numerically, we obtain roughly 0.2 aF and 6 aF for the intrinsic and extrinsic gate capacitances, respectively, where we note that the exact values are functions of the bias, and these quoted values represent the average over our ON-state bias range. While it is well understood that parasitic capacitances become more important as devices are aggressively scaled, the usual intrinsic performance metric does not incorporate these effects. In order to assist in the design of these devices, then, it may be helpful to incorporate these parasitics into the benchmarking process. While a geometry optimization is beyond the scope of this present work, we can place our results in perspective by comparing them with calculations of the extrinsic switching time, as opposed to the intrinsic switching time,[1,3] of present-day silicon MOSFETs. To do this, we performed SPICE simulations for a minimum-size NMOSFET using parameters for a commercially available 90 nm technology.[9] We chose an NMOS silicon device as its higher current drive makes it superior to PMOS devices.[1] In this way, a fair comparison can be made with the CNFETs studied in the present work, which employ Pd end-contacts, which are known to give low barrier heights and, consequently, higher ON currents than are presently possible with so-called n-type CNFETs. Simulations were performed at $V_{DS} = 1\,\text{V}$, for which this technology is optimized, over a V_{GS} range of -1 to $+2\,\text{V}$, from which the $I_{\text{ON}}/I_{\text{OFF}}$ ratio was obtained for $V_{DD} = 1\,\text{V}$. The total gate capacitance, as returned by SPICE as the capacitance C_{GG} at the chosen operating point,

was used to estimate the extrinsic switching time from Eq. (1). The result is shown in Fig. 8. It is clear that this device out-performs the small-diameter, thin-oxide CNFET that appears to be the most practically relevant of the nanotube devices considered here. Typically, the total gate capacitance of the Si FET is around 200 aF, but superior switching performance is achieved by virtue of the higher drive current and the absence of ambipolar conduction. This suggests that a more extensive study of the switching characteristics of CNFETs, involving different geometries and doped-contact-, rather than Schottky-barrier-devices, needs to be performed before any claims can be made as to the superiority of CNFETs over silicon MOSFETs.

IV. CONCLUSIONS

From this simulation study of switching times in Schottky-barrier carbon nanotube FETs it can be concluded that:

1. large-diameter tubes exhibit low intrinsic switching times and poor $I_{\rm ON}/I_{\rm OFF}$ ratios;

2. for small-diameter tubes, the reduction in ON-current, and consequent increase in switching time, can be mitigated somewhat by employing a very thin gate insulator. However, this restricts the range of $I_{\rm ON}/I_{\rm OFF}$ over which low switching times can be realized, due to the onset of carrier injection from the drain;

3. due to the inevitable proximity of the gate and end-contact electrodes, the gate capacitance is dominated by inter-electrode capacitance, which leads to the extrinsic switching time being much longer than the intrinsic switching time;

4. further simulation of CNFET structures is needed to properly assess the switching-speed capabilities of these devices.

Acknowledgement

The support of this work by the Natural Sciences and Engineering Research Council of Canada is gratefully acknowledged. The authors sincerely thank Mr. Derek Ho for assistance with the SPICE simulations.

* Electronic address: pulfrey@ece.ubc.ca

[1] Robert Chau, Suman Datta, Mark Doczy, Brian Doyle, Ben Jin, Jack Kavalieros, Amlan Majumdar, Matthew Metz, and Marko Radosavljevic, IEEE Trans. Nanotechnol. **4**, 153 (2005).

[2] Anisur Rahman, Jing Guo, Supriyo Datta, and Mark S. Lundstrom, IEEE Trans. Electron Devices **50**, 1853 (2003).

[3] Jing Guo, Ali Javey, Hongjie Dai, and Mark Lundstrom, *IEDM Tech. Digest* (2004), pp. 703–706.

[4] Zhihong Chen, Joerg Appenzeller, Joachim Knoch, Yu-Ming Lin, and Phaedon Avouris, Nano Lett. **5**, 1497 (2005).

[5] Ali Javey, Jing Guo, Damon B. Farmer, Qian Wang, Erhan Yenilmez, Roy G. Gordon, Mark Lundstrom, and Hongjie Dai, Nano Lett. **4**, 1319 (2004).

[6] Jing Guo, Supriyo Datta, and Mark Lundstrom, IEEE Trans. Electron Devices **51**, 172 (2004).

[7] D. L. John, L. C. Castro, P. J. S. Pereira, and D. L. Pulfrey, *Tech. Proc. of the 2004 NSTI Nanotechnology Conf. and Trade Show* (Boston, U.S.A., 2004), volume 3, pp. 65–68.

[8] Jijun Zhao, Jie Han, and Jian Ping Lu, Phys. Rev. B **65**, 193401 (2002).

[9] STMicroelectronics, http://www.st.com/stonline/

List of Figures

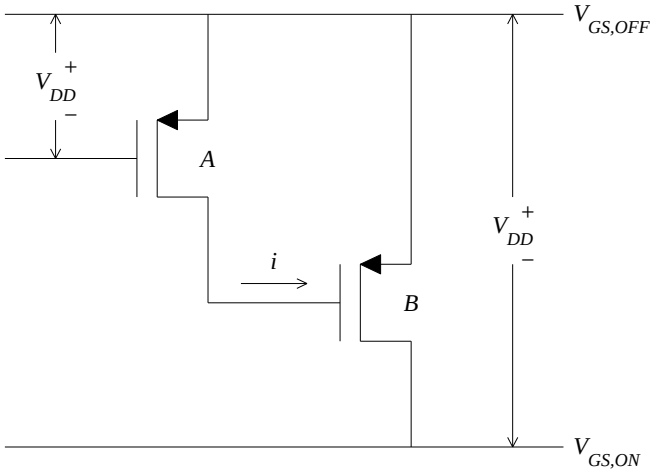

FIG. 1: D. John, Journal of Vacuum Science and Technology

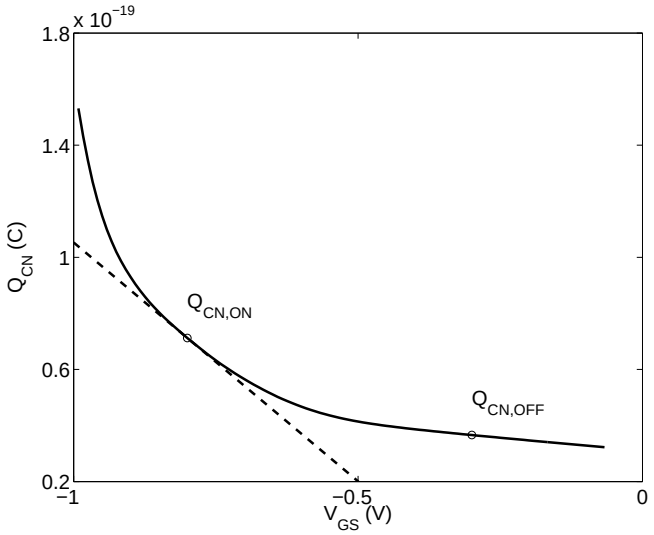

FIG. 2: D. John, Journal of Vacuum Science and Technology

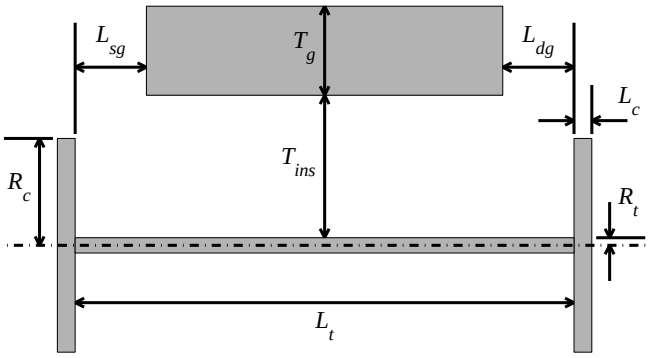

FIG. 3: D. John, Journal of Vacuum Science and Technology

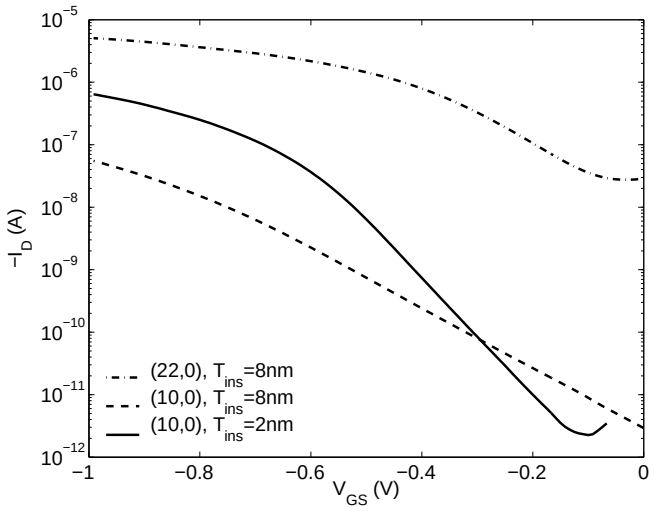

FIG. 4: D. John, Journal of Vacuum Science and Technology

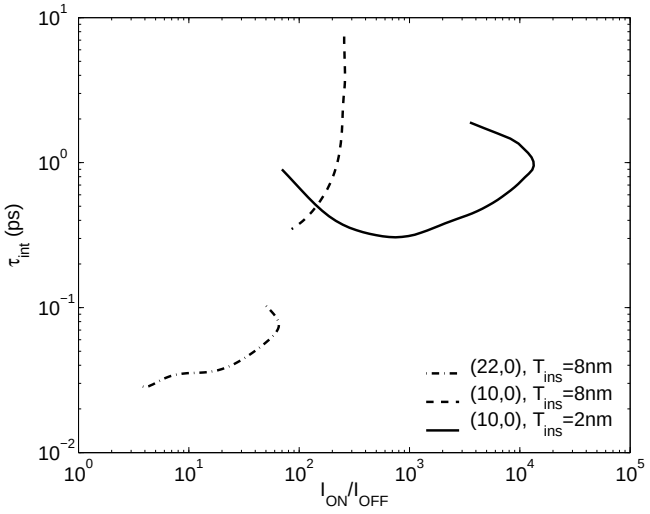

FIG. 5: D. John, Journal of Vacuum Science and Technology

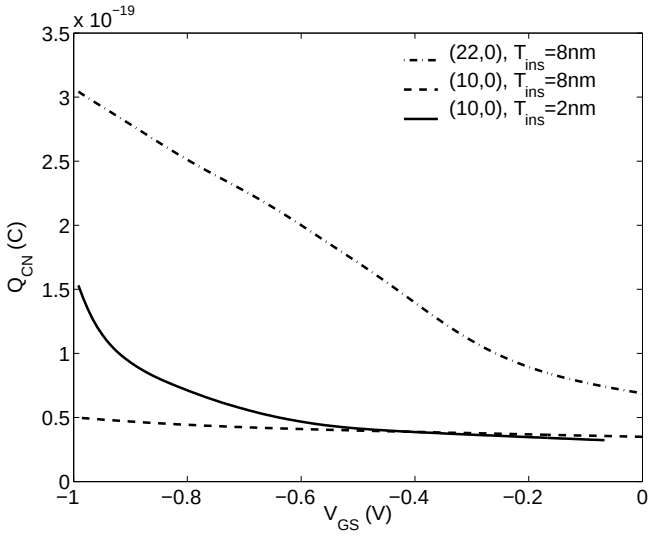

FIG. 6: D. John, Journal of Vacuum Science and Technology

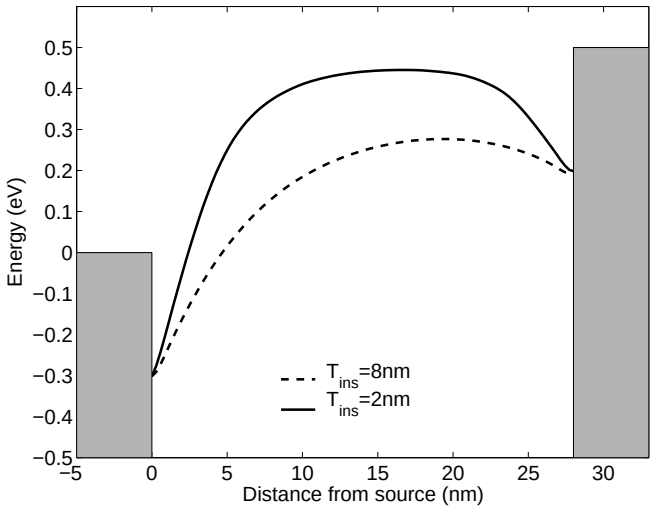

FIG. 7: D. John, Journal of Vacuum Science and Technology

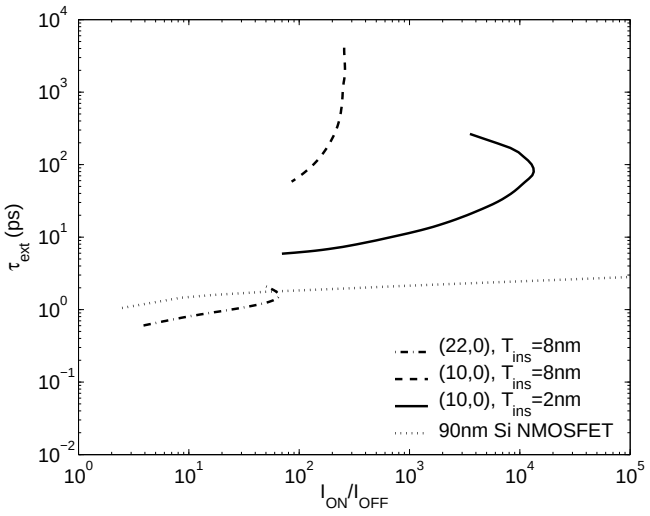

FIG. 8: D. John, Journal of Vacuum Science and Technology