CARBON NANOTUBE TRANSISTORS: AN EVALUATION

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ABSTRACT

A simple, non-equilibrium model is used to evaluate the likely DC performance of carbon nanotube field-effect transistors. It is shown that, by appropriate work function engineering of the source, drain and gate contacts to the device, the following desirable properties should be realizable: a sub-threshold slope close to the thermionic limit; a conductance close to the interfacial limit; an ON/OFF ratio of around 10^3; ON current and transconductance close to the low-quantum-capacitance limit.

Keywords: Carbon nanotubes, field-effect transistors, nanotechnology

1. INTRODUCTION

Carbon nanotube molecules can be either metallic or semiconducting, which raises the fascinating spectre of filamentary integrated circuits fashioned from nanoscale transistors and interconnects.[1] Such circuits would be of a different form from that of today's silicon circuits, and would surely lead to a host of new applications. The atoms within a carbon nanotube molecule bond covalently in hexagonal rings, and this graphite-like structure has great strength and stability. Electrically, this helps in significantly reducing electromigration. This could be an issue as carrier transport in nanotubes is potentially near-ballistic, so operation at high currents is a possibility. Furthermore, carbon nanotubes conduct heat nearly as well as diamond, so extremely high device-packing densities should be possible. When one adds to these advantageous properties the fact that the bandgap of carbon nanotubes can be tuned by varying the tube diameter, then it is clear that carbon nanotubes are worth investigating as candidate molecules for applications in nanotechnology.

The integrity of carbon nanotube molecules may preclude substitutional doping, but adsorbed material,[2] and ions within the nanotube,[3] can alter the tube's conductivity from its natural intrinsic state. Thus, bipolar junction devices are possible, perhaps operating in the single-electron mode with a p-type quantum well between two n-type regions.[2] However, in this paper, we focus on transistors made from intrinsic nanotubes, in which the conductivity is modulated by a gate electrode, *i.e.*, carbon nanotube field-effect transistors (CNFETs). These devices have been under experimental investigation since 1998,[4] and engineering models to aid in their design and analysis are starting to appear.[5–11] Thus, it is timely to assess the performance characteristics of CNFETs, at least under DC operation, for which there is considerable experimental data.

2. FABRICATION

Metallic and semiconducting nanotubes are often sorted on the basis of tube diameter, as measured by atomic force microscopy,[12] but recent reports of covalent chemical functionalization could make this task more practical.[13] Successful attempts to merge metallic and semiconducting nanotubes have been reported,[14] but this desirable union has not yet been incorporated into experimental CNFETs. Instead, these devices presently rely for their fabrication on traditional microelectronic techniques, such as metal deposition and electron-beam lithography, to make and define metal contacts to the nanotube, which forms the channel of the transistor. The nanotubes themselves are either grown *in-situ* by CVD from catalytic island sites,[15] or dispersed from ropes produced by laser ablation of a catalyst-containing carbon target, and positioned on-chip by atomic force

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microscopy.[16] Clearly, if there is to be any hope of mass-production of CNFETs, some method of organized growth, or self-assembly is necessary. Progress in this direction includes aligned growth in an electric field,[17] and growth of arrays of vertical tubes within alumina nanopores.[18]

3. THEORETICAL CONSIDERATIONS

Carbon nanotubes are cylinders of graphene, with a wall thickness of one atomic layer. For small diameter tubes, quantization of the wave vectors in the circumferential (transverse) direction leads to a quasi-one-dimensional energy versus wave vector (E-k) relation, with a continuum of states only in the longitudinal direction. In many cases this entails the opening of a bandgap, which for a 1 nm-diameter tube, for example, is about 0.8 eV. The band structure is usually determined from a tight-binding Hamiltonian, with one p-orbital per carbon atom and a nearest-neighbour matrix element of about 2.8 eV.[19] This approach renders the conduction- and valence-band structures symmetrical. Note that each of the transverse wave vectors corresponds to an allowed mode of propagation, of which there are two in the lowest sub-band, the most relevant in transport calculations.

The small number of propagating modes is in contrast to the very large number of modes in bulk terminals to which a device or circuit must ultimately be connected. This mode-constriction leads to a quantized, interfacial conductance, which exists even if conduction down the nanotube itself is ballistic.[20] In the modeling of carbon nanotube diodes and field-effect transistors, it is becoming customary to locate such interfaces at the end contacts to a semiconducting nanotube, and to regard the nanotube as an object with a characteristic transmission probability $\mathcal{T}$.[7, 11, 21] The end contacts are viewed as reservoirs of charge, maintained under equilibrium conditions, from which carriers are injected into the nanotube, depending on $\mathcal{T}$ and the applied bias, *e.g.* the drain-source voltage V_{DS} of a CNFET. This Landauer formalism, as described by Datta,[20] allows the net electron current for two modes to be expressed as

$$I_e = \frac{4q}{h} \int_{E_{C,\mathrm{mid}}}^{\infty} \mathcal{T}_e(E)[f(E) - f(E + qV_{DS})]\, dE\,, \tag{1}$$

where q is the magnitude of the electronic charge, h is Planck's constant, $E_{C,\,\mathrm{mid}}$ is the energy of the conduction band edge in the mid-section of the nanotube, $f(E)$ is the Fermi-Dirac distribution function, and $\mathcal{T}_e$ refers to electrons. Clearly, the lower limit of integration would need to be changed if source-drain tunneling were an issue. A similar expression can be written for holes, using a transmission probability $\mathcal{T}_h$. Thus, once the $\mathcal{T}$'s are known, the problem of the DC drain current is solved.

4. DC MODELING

Present CNFETs are usually planar devices, with a single gate situated either above,[22] or below,[16] the gate dielectric and the nanotube. Double-gated devices,[23] and electrolytically gated devices,[24] more closely resemble the coaxial structure with wrap-around gate that would be ideal, given the cylindrical form of the nanotube. As we are interested in ultimate-performance assessment, we take a coaxial geometry for modeling purposes, as illustrated in Fig. 1. If the source and drain end contacts are the same radius as the gate, a closed metallic cylinder results, for which there is an analytical solution for the device electrostatics.[8] For smaller diameter end contacts, or for partially gated devices in which the gate electrode does not cover the entire length of the nanotube, an open-boundary problem exists, and numerical methods need to be employed.[10, 25]

The transmission probabilities $\mathcal{T}$ are functions of energy and local potential $V(\rho, \phi, z)$. The latter is related to charges within the system, such as: electrons, holes and adsorbed ions on the nanotube; charges trapped within the gate dielectric or the nanotube; charges residing in so-called metal-induced-gap-states (MIGS), or evanescent states within the semiconductor bandgap near the junctions. Here, we consider only electrons and holes, which are taken to reside on the surface of the tube, *i.e.*,

$$Q(\mathbf{r}) = \frac{1}{2\pi\rho}\delta(\rho - R_T)Q_z(z)\,, \tag{2}$$

where $Q_z(z)$ is the charge due to the net 1-D carrier concentration, R_T is the nanotube radius, and $\delta(x)$ is the Dirac delta function.

If we allow for a spatially varying permittivity in the radial direction, Gauss' Law implies that:

$$\frac{\partial^2 V}{\partial \rho^2} + \left(\frac{1}{\rho} + \frac{1}{\epsilon} \frac{\partial \epsilon}{\partial \rho} \right) \frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q(\mathbf{r})}{\epsilon}, \tag{3}$$

where the potential within the device reduces to a function of just two cylindrical coordinates $V(\rho, z)$, due to the symmetry of the device in the angular direction. The charge $Q_z(z)$ is distributed within the allowed 1-D density-of-states (DOS), which is taken to be rigidly shifted by $V(\rho, z)$.

The solution for the potential is relatively straightforward under equilibrium conditions because Fermi-Dirac statistics apply not just in the metal contacts, but everywhere along the tube, and can be used to compute the electron and hole concentrations.[8] In the absence of gate leakage, equilibrium occurs when $V_{DS} = 0$.

Out of equilibrium in the sub-threshold region of operation or even, as it has been claimed, in the turn-on mode,[26] $Q_z(z)$ may be so small that it can be set to zero, and a solution to Laplace's equation can be used for $V(\rho, z)$.

In the fully-on state, $Q_z(z)$ cannot be ignored. In the earliest CNFET model, this charge was taken to maintain its equilibrium value,[5] as would be appropriate for a FET working in the traditional, charge-control mode.[27] Because of the large insulator capacitance, and small quantum capacitance, that can be obtained in CNFETs (see next section), a voltage-controlled mode of operation is more relevant for these devices,[27] at least when tunneling is not important. In this mode, it is the mid-tube potential energy $E_{C,\mathrm{mid}}$ that is important because it controls the height of the barriers to thermionic emission at the end contacts. This potential energy is solved for self-consistently with the mid-length charge in a recent model,[7] which has been extended here to account for both electron and hole charge and transport. In this model, $E_{C,\mathrm{mid}}$ is connected to the end-contact barrier heights using a compact expression for the potential profiles based on solutions to Laplace's equation. Obviously, this will only give approximate results in cases where the actual shape of the barrier is important, but it will give good results in devices where it is only the height of the barrier that is important, as in, for example, metal/nanotube junctions with a negative barrier height for electrons, or doped/intrinsic nanotube junctions. This method was used to obtain the results presented here.

Another approach is to employ quasi-equilibrium statistics, with a separate quasi-Fermi level for each sub-band. In the case of ballistic transport, the quasi-Fermi levels are flat along the length of the tube, and they split at the end contacts. A flux-balancing approach can then be used to include the current, as well as the charge and the potential, in a self-consistent solution.[9]

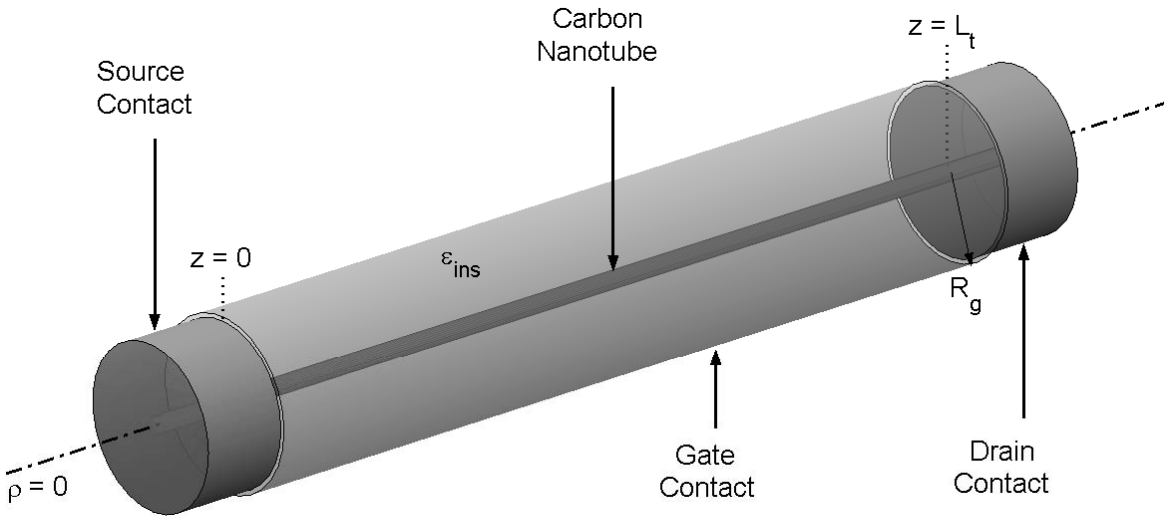

Figure 1. The coaxial CNFET structure.

The shortcoming of any semi-classical model is that, while the non-equilibrium electron and hole concentrations within the allowed bands may be computed, allowance is not made for charge in evanescent states. However, if this charge does not lead to a change in the mid-tube potential energy $E_{C,\mathrm{mid}}$, then the neglect of it will not affect the computation of the salient thermionic emission current.

A full, quantum-mechanical, approach is necessary to achieve a complete solution in cases where the charge in evanescent states is important, and where tunneling Schottky barriers are present, and in all devices where resonance and coherency are issues, and also where source-to-drain tunneling is a possibility.[11]

Irrespective of the independent method used to compute $Q_z(z)$, Eq. (3) needs to be solved subject to the appropriate boundary conditions. Conformal mapping is effective when open boundaries are present.[25] For the metallic electrodes, a simple phenomenological representation, assuming no Fermi-level pinning,[21] is

$$\begin{aligned} V(R_G, z) &= V_{GS} - \Phi_G/q \\ V(\rho, 0) &= -\Phi_S/q \\ V(\rho, L) &= V_{DS} - \Phi_D/q\,, \end{aligned} \tag{4}$$

where Φ_G, Φ_S and Φ_D are the work functions of the gate-, source- and drain-metallizations, respectively, and V_{GS} is the gate-source voltage. Recent experimental results, which show a strong dependence of device characteristics on metal work function, indicate that this phenomenological representation of the contacts may be appropriate.[28]

5. RESULTS AND DISCUSSION

In this section we wish to evaluate the following properties of CNFETs: ambipolarity, high conductance, geometry-dependent sub-threshold slope, high ON-current and transconductance.

A closed, coaxial geometry is used, with a gate dielectric of thickness 2.5 nm and a relative permittivity of 25, as is appropriate for zirconia, which has been employed in some CNFETs.[22] An intrinsic (16,0) nanotube is used, for which the radius, bandgap and electron affinity are 0.63 nm, 0.64 eV and 4.2 eV, respectively.[4] The tube length is taken to be 20 nm, which should ensure that transport is ballistic over the bias range considered.[29] The effect of changing the work functions for all three electrodes is examined. The values chosen are 4.5, 4.2 and 3.9 eV, corresponding, in the case of the source/drain electrodes, to barriers for electrons at the metal/nanotube interfaces that are positive, zero, and negative, respectively. These electron barrier heights are given by the difference between the metal work function and the nanotube electron affinity, *i.e.*, $\Phi_{Bn} = \Phi_M - \chi_{CN}$. All simulations are performed for a temperature of 300 K.

5.1. Ambipolarity

Ambipolarity refers to the fact that, under certain bias conditions, channel conduction in CNFETs is due to either electrons or holes.[30] Thus, depending on the bias, a particular CNFET may be either "n-type" or "p-type". The situation is illustrated in Fig. 2 for a CNFET with positive barrier end contacts. In this case $\Phi_{Bn} = E_g/2$, where E_g is the nanotube bandgap. The figure shows that, for a constant V_{DS}, the conduction can be due to either electrons or holes, depending on the gate bias V_{GS}. In this case, at $V_{GS} - \Phi_G/q = V_{DS}/2$, the electron and hole currents are equal, and the total current attains its minimum value,[8] as can be seen on the I_D-V_{GS} plot in Fig. 3. Ambipolarity is an undesirable feature in FETs because it leads to an unwanted OFF current at $V_{GS} = 0$. Fig. 3a shows that, while a negative barrier end contact can reduce the minimum current, it offers no advantage over a zero-barrier end contact as regards reducing I_{OFF}. This is because at zero gate bias $E_{C,\mathrm{mid}}$ is determined only by Φ_G, and so the same barrier height is presented to the thermionic currents in the two cases (see Fig. 4). The OFF current is smaller in the positive-barrier case because of tunneling. Work function engineering of the gate metal can be used to laterally shift the I-V curves so that the minimum current occurs at $V_{GS} = 0$ (see Fig. 3b). Even though the higher $E_{C,\mathrm{mid}}$ that brings this about also reduces the ON current, the ON/OFF ratio is improved. Clearly, there is opportunity for creative work function engineering here, and an ON/OFF ratio of around 10^3 would appear to be possible.

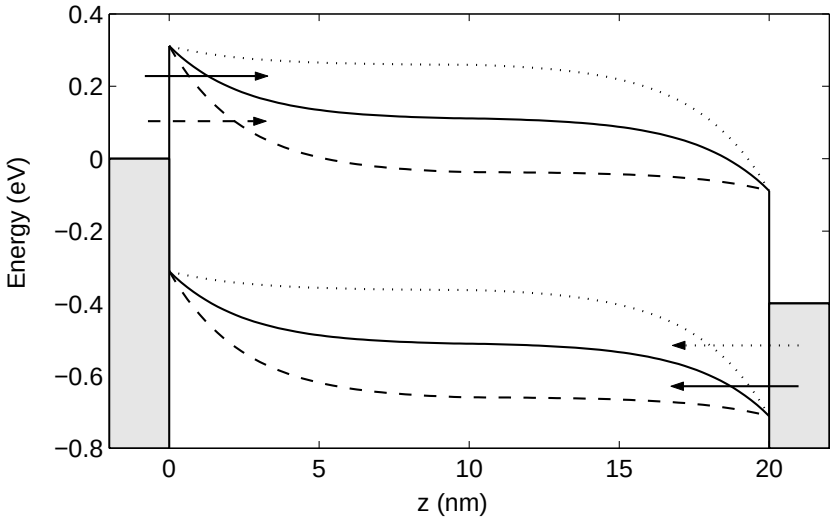

Figure 2. Band diagram illustrating ambipolarity in a device with $\Phi_G = \Phi_{S,D} = 4.5\,\mathrm{eV}$, $V_{DS} = 0.4\,\mathrm{V}$. Hole injection at $V_{GS} = 0.05\,\mathrm{V}$ (dotted line and arrow); electron and hole injection at $V_{GS} = 0.2\,\mathrm{V}$ (solid line and arrows); electron injection at $V_{GS} = 0.35\,\mathrm{V}$ (dashed line and arrow).

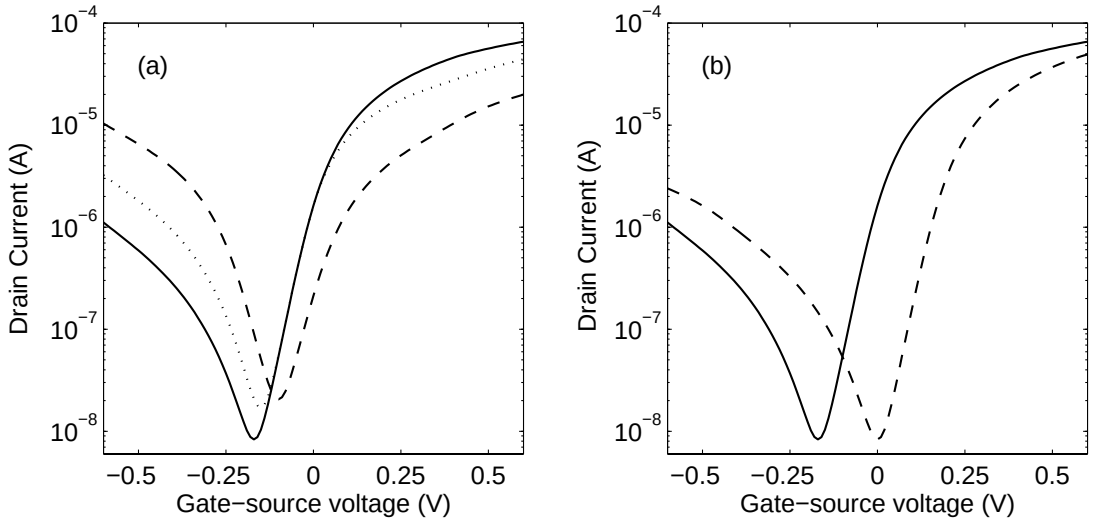

Figure 3. I_D-V_{GS} at $V_{DS} = 0.4\,\mathrm{V}$. (a) $\Phi_G = 4.2\,\mathrm{eV}$ and various $\Phi_{S,D}$: 3.9 (solid line); 4.2 (dotted line); 4.5 eV (dashed line). (b) $\Phi_{S,D} = 3.9\,\mathrm{eV}$: $\Phi_G = 3.9$ (solid line), and $\Phi_G = 4.37\,\mathrm{eV}$ (dashed line).

5.2. Conductance

The quantized interfacial conductance, as mentioned earlier, has a maximum value $G_{\max} = 4q^2/h$ for a nanotube with two transverse modes.[20] Measurements of conductance, $G = I_D/V_{DS}$, can only be expected to approach $G_{\max}$ for ballistic transport in nanotubes with end contacts that have neither ohmic- nor tunneling-resistance. Ballistic transport demands measurement at low V_{DS} to avoid exciting optical phonons at higher biases, and a nanotube length that is less than the mean-free-path for acoustical phonon scattering (about 300 nm).[29] Using devices of about this length with Pd end contacts, which yield low-resistance contacts with near-zero barrier height for holes, impressive values of $G \approx 0.4G_{\max}$ have been reported already.[28]

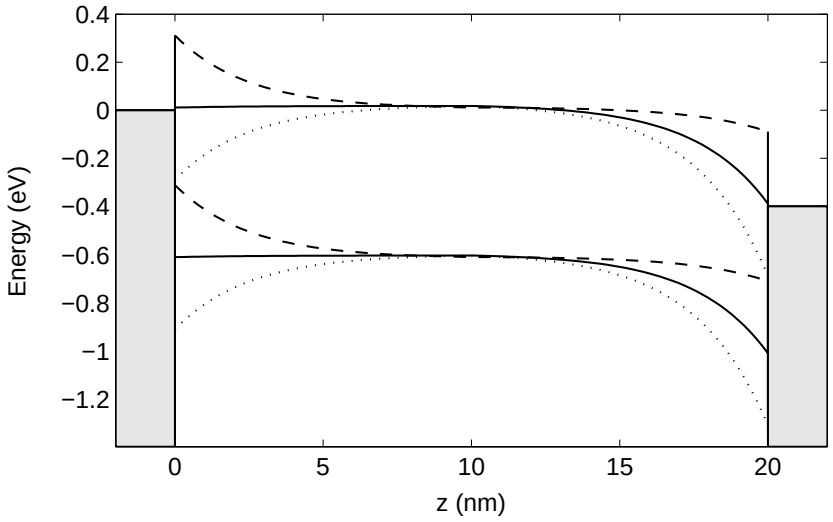

Figure 4. Band diagrams at $V_{GS} = 0$ and $V_{DS} = 0.4\,\mathrm{V}$ for the three devices used in Fig. 3a. $\Phi_G = 4.2\,\mathrm{eV}$ and various $\Phi_{S,D}$: 3.9 (dotted line); 4.2 (solid line); 4.5 eV (dashed line).

5.3. Subthreshold slope

The limiting value for the sub-threshold slope S, in situations where the sub-threshold current is thermionically determined, is about $60 m_Q\,\mathrm{mV/decade}$, where $m_Q = 1 + C_Q/C_{\mathrm{ins}}$ is the "quantum capacitance coefficient", with C_Q being the quantum capacitance,[5] and C_{ins} the insulator capacitance. The use in CNFETs of high-permittivity dielectrics, such as zirconia[22] or aqueous solutions,[24] opens up the possibility of attaining values of m_Q approaching unity. Thus, near-minimum values of S would be expected to be approached in CNFETs with negative barrier heights at the end contacts. Higher values can be expected for positive barrier heights due to the presence of tunneling barriers. However, if these barriers are rendered essentially transparent by a suitable gate bias, then values of S in these devices should also approach the thermionic limit. In all cases, because the injecting barrier is modulated by the gate voltage via capacitive coupling, S will show a dependence on the gate/channel geometry.[8, 23] For CNFETS with positive barrier-height end contacts and $t_{\mathrm{ox}} = 2\,\mathrm{nm}$, for example, $S = 110\,\mathrm{mV/decade}$ has been measured for planar CNFETs,[23] and $S \approx 80\,\mathrm{mV/decade}$ has been predicted for coaxial devices, in which the capacitive coupling is superior. For a SiO_2 gate oxide with $t_{\mathrm{ox}} = 67\,\mathrm{nm}$, and tubes contacted with palladium, planar devices have been reported with $S \approx 150\,\mathrm{mV/decade}$.[28] With a thinner insulator of higher permittivity,[22] it is likely that Pd-contacted CNFETs will attain values of S very close to the theoretical limit.

5.4. ON Current

For maximizing the ON current, tunneling barriers must be avoided, and electron injection from the drain must be suppressed. This situation can be simulated by using a high-enough V_{DS} in Eq. (1) and setting $\mathcal{T} = 1$, which also implies neglecting quantum-mechanical reflection at the metal/nanotube interfaces. Integrating Eq. (1) then leads to

$$I_{e,\max} = \frac{4q}{h} kT \ln\left[1 + \mathrm{e}^{-\frac{E_{C,\mathrm{mid}}}{kT}}\right] . \tag{5}$$

This equation would be more useful if $E_{C,\mathrm{mid}}$ were converted to an independent parameter, such as V_{GS}. The relationship between these two quantities for an intrinsic nanotube is

$$E_{C,\mathrm{mid}} = \frac{E_g}{2} - \left[\frac{qV_{GS} + \Delta\Phi}{m_Q}\right] , \tag{6}$$

where $\Delta\Phi$ is the difference in work function between the nanotube and the gate metal. Note that the relationship would be essentially linear if $C_Q \ll C_{\rm ins}$, *i.e.*, in the "quantum-capacitance limit" of $m_Q = 1$. This inequality can be readily examined in the mid-tube region, where C_Q is given by $-dQ_z/dE_{C,\rm mid}$ and is easily computed at equilibrium. The result is shown in Fig. 5, from which it is clear that $C_Q \ll C_{\rm ins}$ only at low bias, *i.e.*, when there is very little charge in the nanotube. However, if one allows this inequality to hold to higher bias,[27] then Eq.(5) reduces to a linear form in which the control by V_{GS} is obvious. Such a result is plotted from Eqs. (5) and (6) in Fig. 6a, where the solid line sets an upper limit to the unipolar current. As a reality check, the maximum drain current that has been measured so far in a CNFET is about $25\,\mu$A.[28] Much higher values should be possible with appropriate work function engineering, as shown by the simulation results of Fig. 7. Low electron

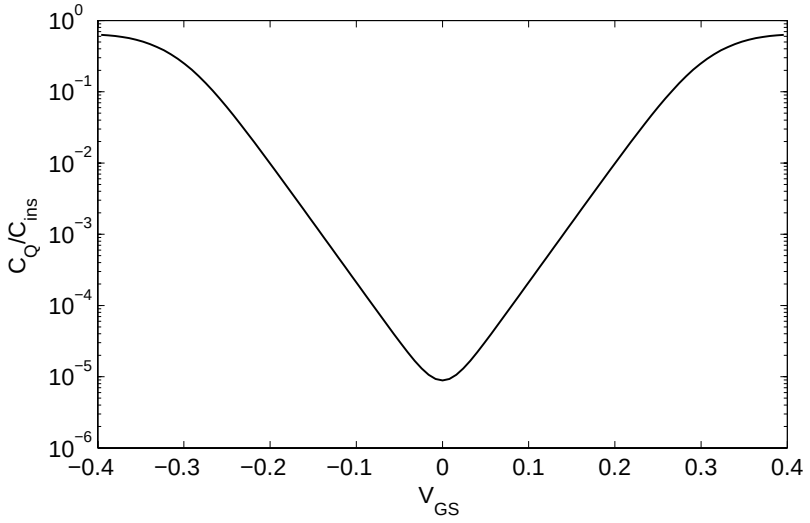

Figure 5. Ratio of equilibrium quantum capacitance to insulator capacitance for an insulator relative permittivity and thickness of 25 and 2.5 nm, respectively, and for all work functions equal to 4.5 eV.

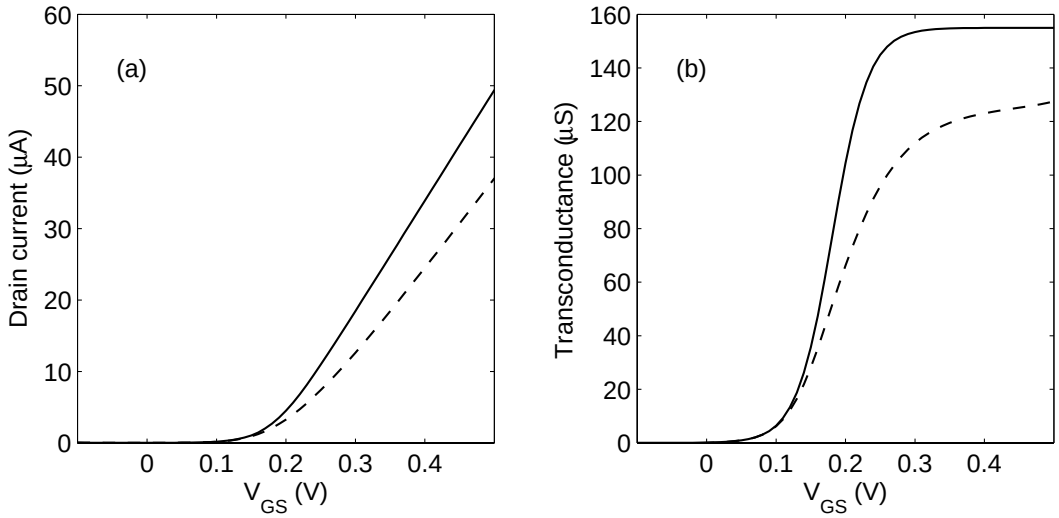

Figure 6. (a) I_D, and (b) g_m, as a function of gate-source voltage. The solid lines are for the "quantum-capacitance limit" from Eqs. (5), (6) and (7). The dashed lines are for a device with $\Phi_{S,D} = 3.9\,$eV and $\Phi_G = 4.37\,$eV, *i.e.*, the device that gave the lowest OFF current in Fig. 3.

barriers at the end contacts give high currents (see Fig. 7a), which can be further enhanced at a given gate bias by reducing the gate work function (see Fig. 7b).

The effect of Φ_G is examined in the band diagrams of Fig. 8, which illustrate the case of $V_{GS} = V_{DS} = 0.4\,\mathrm{V}$. At $\Phi_G = 3.9\,\mathrm{eV}$, $E_{C,\mathrm{mid}}$ is depressed to the extent that a tunneling barrier forms for the low energy electrons in the source. With low Φ_G, clearly a larger V_{DS} is required to suppress the drain-injected electron current, leading to a higher saturation voltage $V_{DS,\mathrm{sat}}$. In the example shown in Fig. 7b this could be an issue if CNFET logic circuits were constrained to operate at 0.4 V, which is the power-supply voltage specified for 10 nm-scale Si MOSFETs.[31] Note that the hole barriers in all cases are too high for ambipolar effects to be seen at the bias values considered here. Thus, the drain characteristics are of the traditional "saturating" variety, with no rapid rise due to hole injection, as has been observed in some experimental data,[32] presumably due to the use

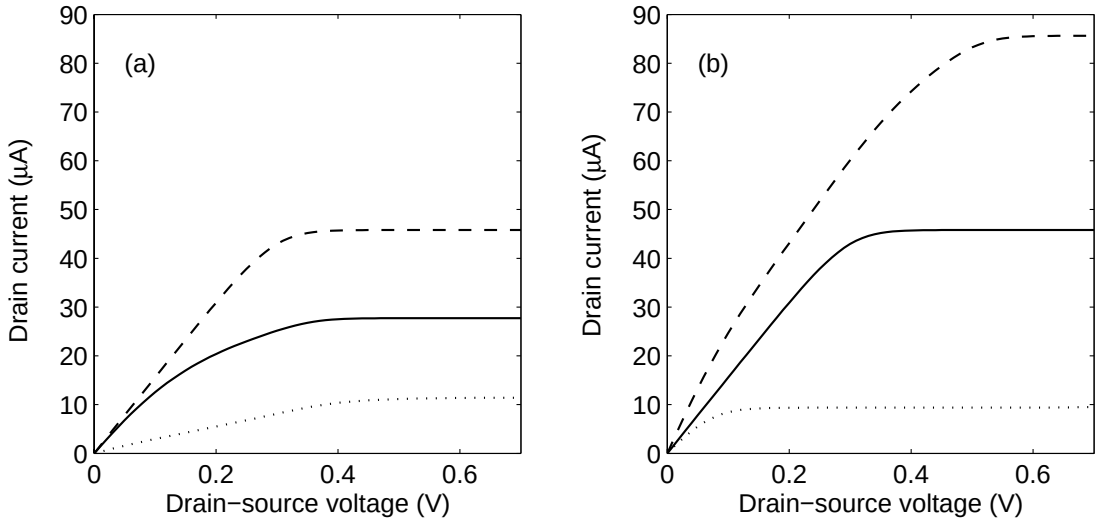

Figure 7. Drain characteristics at $V_{GS} = 0.4\,\mathrm{V}$. (a) $\Phi_G = 4.2\,\mathrm{eV}$ and $\Phi_{S,D} = 3.9$ (dashed line); 4.2 (solid line); and 4.5 eV (dotted line). (b) $\Phi_{S,D} = 3.9\,\mathrm{eV}$ and $\Phi_G = 3.9$ (dashed line); 4.2 (solid line); and 4.5 eV (dotted line).

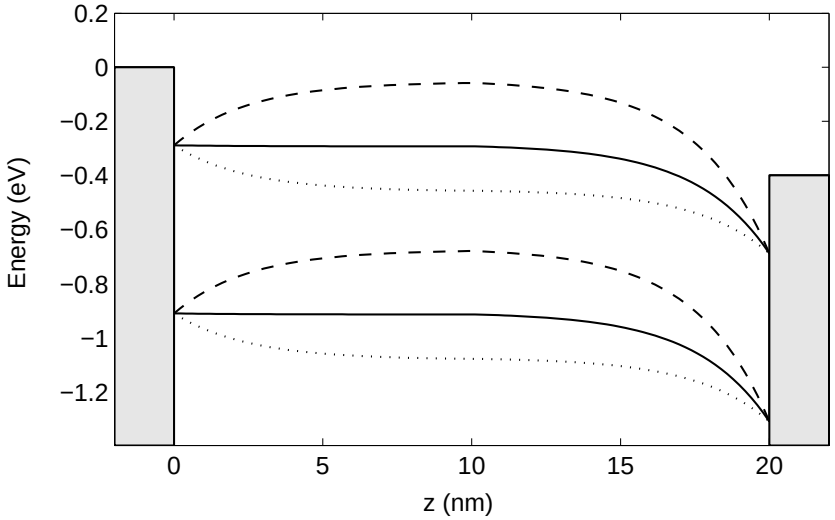

Figure 8. Band diagrams for various Φ_G at $\Phi_{S,D} = 3.9\,\mathrm{eV}$ and $V_{GS} = V_{DS} = 0.4\,\mathrm{V}$: $\Phi_G = 3.9$ (dotted line); 4.2 (solid line); and 4.5 eV (dashed line).

of positive-barrier end contacts.[9]

In view of the fact that a CNFET with high ON current should also have a low OFF current, we compute I_D for the case of $\Phi_G = 4.37\,\text{eV}$ and $\Phi_{S,D} = 3.9\,\text{eV}$, which led to the low OFF current shown in Fig. 3b. The result is shown in Fig. 6a. It can be seen that at $V_{DS} = 0.4\,\text{V}$, I_D is about 80% of the ultimate value. Finally, it is noteworthy that the highest drain current shown in Fig. 7b is equivalent to a current density ($I_{D,\max}/2R_T$) of about $70\,\text{mA}/\mu\text{m}$!

5.5. Transconductance

The limit to the attainable transconductance can be obtained from the differentiation of Eq. (1), which, in the quantum-capacitance limit, yields

$$g_{m,\max} = \frac{4q^2}{h}\left[1 + \exp\left(\frac{1}{kT}\left(\frac{E_g}{2} - qV_{GS} + \Delta\Phi\right)\right)\right]^{-1} \tag{7}$$

As Fig. 6b reveals, at high V_{GS}, $g_{m,\,\max}$ attains its limiting value of $4q^2/h$, which, interestingly, is the same value attainable by $G_{\max}$, as noted elsewhere.[33] Taking once more the device with $\Phi_G = 4.37\,\text{eV}$ and $\Phi_{S,D} = 3.9\,\text{eV}$ as an example, at $V_{DS} = 0.4\,\text{V}$, a value of g_m close to 80% of the ultimate value is indicated.

6. CONCLUSIONS

From this evaluation of the DC performance of carbon nanotube field-effect transistors, it can be concluded that in n-type devices, for example, the use of negative barrier-height source and drain contacts, and low work function gate metallization, should allow attainment of sub-threshold slopes, conductances, transconductances and ON currents close to the ultimate limits. These features, allied to the excellent thermal and mechanical properties of carbon nanotubes, make these molecules strong contenders for implementation in nanoscale integrated circuits.

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