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Examination of the high-frequency capability of carbon nanotube FETs

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ABSTRACT

New results are added to a recent critique of the high-frequency performance of carbon nanotube field-effect transistors (CNFETs). On the practical side, reduction of the number of metallic tubes in CNFETs fashioned from multiple nanotubes has allowed the measured f_T to be increased to 30 GHz. On the theoretical side, the opinion that the band-structure-determined velocity limits the high-frequency performance has been reinforced by corrections to recent simulation results for doped-contact CNFETs, and by the ruling out of the possibility of favourable image-charge effects. Inclusion in the simulations of the features of finite gate-metal thickness and source/drain contact resistance has given an indication of likely practical values for f_T. A meaningful comparison between CNFETs with doped-contacts and metallic contacts has been made.

1. Introduction

This invited paper provides an opportunity to update a critique of the high-frequency performance of CNFETs presented at ESSDERC-07 [1]. The focus is on the short-circuit, common-source, unity-current-gain frequency, f_T. The existing measured data is collected, and a new record value is reported [2]. The existing simulation results for Schottky-barrier (SB) CNFETs are collected, and grouped such that the effects on f_T of the following factors can be clearly seen: oxide permittivity, tube chirality, extrinsic capacitance, contact size and resistance, phonon scattering. New simulation results for doped-contact n–i–n CNFETs are added to the data presented in Ref. [1]; they show the effect on f_T of: tube chirality, gate length, gate-metal thickness, and contact resistance. Importantly, correction of some earlier data, which suggested an extraordinarily high f_T capability [3,4], has been noted [5].

It is now observed that all the simulation results for both SB- and doped-contact-CNFETs fall below the limit imposed by the propagation velocity of electrons in the gated region of the nanotube [6]. This may seem like an obvious result; however, its application to nanoscale FETs needs to be re-asserted for at least two reasons: firstly, to dispel doubts caused by earlier simulation results [3,4]; secondly, to re-affirm that "image-charge" effects, which can lead to signal delay times being shorter than propagation delay times in field regions of bipolar transistors, are not significant in nanoscale FETs [7], even though a pronounced field can exist in the gated region of doped-contact CNFETs [8].

2. Experimental results

The low current-drive and high input/output impedance of single CNFETs make it difficult to perform direct measurements of high-frequency electrical properties, at least when using instrumentation based on a reference impedance of 50 Ω. In order to make a direct measurement of a recognized high-frequency figure-of-merit, such as f_T, it has been realized that CNFETs assembled from multiple nanotubes must be employed [2,9–11]. Such measurements are in their infancy, and problems of non-parallel nanotubes, the presence of some metallic nanotubes, and excessive gate overlap capacitance need to be addressed. However, progress is being made, and the highest f_T recorded thus far, after de-embedding, is 30 GHz [2]. The experimental data is shown in Fig. 1; there is some dependence on gate length L_G, which is indicative of the success of the de-embedding procedures employed to negate the effect of the pad parasitics. The figure also shows the gate-length dependence of f_T, as predicted in the "ultimate" limit of the signal delay being determined solely by the propagation of electrons through the gated portion of the nanotube [6]. Satisfaction of this condition is equivalent to having no charge change (capacitance) associated either with regions of the CNFET external to the gated-portion, or with parasitic structures. Clearly, such an ideal situation cannot be attained in practice, but the comparison emphasizes that effort should be put into making measurements on structures using shorter nanotubes. Certainly, as Fig. 1 also shows, shorter channel lengths or basewidths have been employed to obtain record f_T values for other types of transistor: Si MOSFETs (330 GHz [12]) and InP/InGaAs HBTs (710 GHz [13]).

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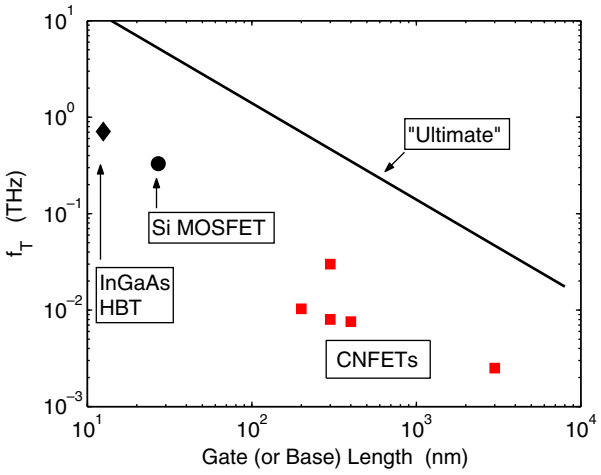

Fig. 1. Experimental data from high-frequency transistors. CNFETs – squares [2,9–11]; SiCMOS – circle [12]; HBT – diamond [13]; and the "ultimate" curve is from Eq. (1).

The ultimate limit, referred to above, proposes

$$2\pi f_{T,\text{ultimate}} = \frac{v_{b,\text{high}}}{L_G}, \tag{1}$$

where $v_{b,\text{high}}$ is the maximum, band-structure-limited velocity that can be attained. In the zig-zag nanotubes considered here, the value of $v_{b,\text{high}}$ depends on the choice of the overlap parameter used in the tight-binding approximation to get the band structure. Here we use 2.8 eV, which gives the maximum velocities listed in Table 1 for various tubes. Note that the maximum propagation velocity in the carbon nanotubes is attained around 1 eV above the edge of the first conduction sub-band, and, consequently, is only likely to be reached by electrons injected into a region of high electric field. The "ultimate" line in Fig. 1 is drawn for $v_{b,\text{high}} = 8.8 \times 10^5$ m/s: this value gives a convenient figure for $f_{T,\text{ultimate}}$ in THz of $140/L_G$, with L_G in nm. This number is indicative of a fundamental limit, as opposed to a phenomenological limit, for which one proposed value is $80/L_G$ [16].

3. Simulation results

Detailed theoretical analyses involve the self-consistent solution of the equations of Schrödinger and Poisson, usually under the quasi-static approximation [17], which is appropriate as f_T is a parameter attained by extrapolation from lower frequencies.

Table 1
Maximum band-structure-limited velocity, and the energy above the edge of the first conduction sub-band at which it is attained

Material	Chirality	Bandgap (eV)	$E_{v_{b,\text{high}}} - E_C$ (eV)	Maximum velocity (10^5 m/s)
C NT	10,0	0.98	1.22	9.1
C NT	11,0	0.95	1.06	7.5
C NT	13,0	0.76	1.11	9.1
C NT	14,0	0.74	1.00	7.9
C NT	16,0	0.62	1.03	9.1
C NT	17,0	0.61	0.96	8.1
C NT	19,0	0.52	0.96	9.1
C NT	20,0	0.51	0.89	8.2
C NT	22,0	0.45	0.90	9.1
Si NW		2.85	≈0.6	≈5.8
InAs NW		0.48	≈0.18	≈4.5

The Si data is for a [100] nanowire of diameter 1.36 nm, as inferred from data in Ref. [14]. The InAs data is for a [100] nanoribbon of cross-section 13×13 nm^2, as inferred from data in [15].

Methods involving either an effective-mass wave equation, or a Hamiltonian based on atomistic considerations, have been employed, and, under suitably low-bias conditions, should give similar results [18], provided the simulation space is properly bounded [19].

The extrapolated f_T is given by

$$2\pi f_T = \frac{\partial I_D}{\partial Q_G} \equiv \frac{g_m}{C_{Gi} + C_{Ge}}, \tag{2}$$

where ∂I_D and ∂Q_G are changes in output (drain) current and input (gate) charge, respectively, due to a change in gate-source voltage, for example; g_m is the transconductance, and C_{Gi} and C_{Ge} are contributions to the total gate capacitance C_{GG} arising from the region under the gate (intrinsic), and the gate-electrode regions (extrinsic), respectively.

3.1. Schottky-barrier CNFETs

Fig. 2 is illustrative of the coaxial, all-around-gate structure that is usually used in simulations of SB-CNFETs [20]. The results that have been obtained for simulation of SB-CNFETs are collected together in Fig. 3. The data labeled C_{Ge} comes from two devices of different gate length and underlaps [20,21]: for the $L_G = 2$ nm case (solid diamonds), the effect is large because of the small gate-source underlap L_{uS} (14 nm); in the $L_G = 5$ nm case (open diamonds), increasing the separation of source and drain electrodes

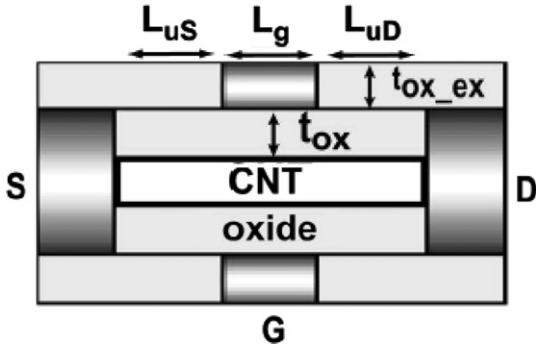

Fig. 2. Coaxial Schottky-barrier CNFET with wrap-around gate, showing some of the pertinent structural parameters [20].

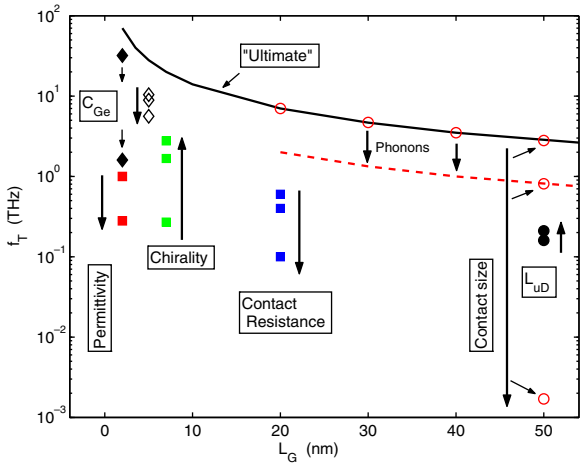

Fig. 3. Summary of simulation results for SB-CNFETs. Effect of various parameters on f_T: C_{Ge} [20,21]; oxide permittivity and nanotube chirality [22]; contact resistance [23]; contact size [24]; gate-drain underlap [25]; phonon scattering [26]. Arrows indicate increasing parameter.

(L_{uS} and L_{uD}) to 24 nm mitigates the effect. The results shown are for contact radii varying from that of the nanotube itself, to that of the nanotube plus oxide and gate thicknesses [21]. The beneficial effect of increasing L_{uD} (from 5 to 25 nm) is also shown by the solid-circle data at $L_G = 50$ nm [25]. The open-circle data at $L_G = 50$ nm comes from a planar structure [24]; the degradation of f_T is again related to an increase in C_{Ge}, and is due to changing the contact from that of a needle of radius equal to that of the nanotube, to that of a metallic strip of width 8 μm. The latter was the actual electrode structure of a high-performance DC device [27], and emphasizes the need to develop finer contact arrangements for HF devices. It is clear that C_{Ge} has a large effect on the performance of these nanoscale transistors, and it must be included in simulations if predictions of f_T are to be meaningful [28].

The square data points at $L_G = 2$ nm show the effect of increasing ϵ_{ox} from 3.9 to 25 while keeping the insulator thickness fixed at 2.5 nm [22]. The point of these two simulations was to assess the trade-off between increased C_{Gi} (there were no underlaps) and increased g_m due to the stronger electrostatic coupling between gate and nanotube. Evidently, the effect of the capacitance is greater, so f_T decreased. For Schottky-barrier contacts representing palladium, the barrier height for hole injection decreases as the nanotube chirality (and diameter) increases [29]. This enhances g_m, leading to the improved performance shown in Fig. 3 on changing the chirality from (11,0) (diameter = 0.8 nm) through (16,0) to (22,0) (diameter = 1.7 nm) [22]. Fig. 3 also shows the effect of considering the actual resistance of the source and drain contacts. Such resistances can be expected to be high when employing nanoscale needle contacts. The results shown are for $R_{contact}$ increasing from zero through 10–100 kΩ [23]. Similar degradations also apply to f_{max} [30]. Phonon scattering could be important, at least in tubes of length greater than about 10–20 nm, which is the mean-free-path for optical phonons [26]. The effect is illustrated by the downward shift of the "ultimate" line to that of the dashed line shown in Fig. 3 [26]. Phonon scattering leads to a build-up of charge in the channel, i.e. to an increase in C_{Gi}.

3.2. Doped-contact CNFETs

In addition to coaxial structures akin to those in Fig. 2, double-gate structures, of the form shown in Fig. 4 [3,4], have been used in the simulation of doped-contact-CNFETs. The results that have been obtained for simulation of doped-contact-CNFETs are collected together in Fig. 5. Earlier, very high, f_T results for double-gate

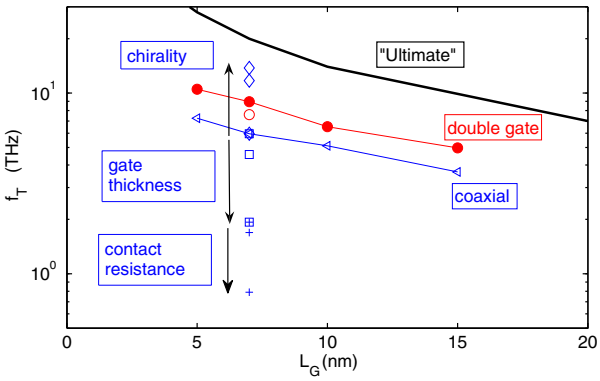

Fig. 5. Summary of simulation results for doped-contact-CNFETs. Double-gate devices: filled circles [5], open circle [31]. Coaxial devices – diamonds, squares, triangles, and crosses [32].

structures [3,4] have now been corrected [5], bringing them into good agreement with results from other workers [31]. All data shown are for (11,0) nanotubes. Results for a coaxial geometry using the same tube are also shown in Fig. 5 [32]. The slightly inferior performance of the coaxial devices is due principally to the increased capacitance that results from this geometrical arrangement. The beneficial effect of increasing the chirality (from (11,0) through (16,0) to (22,0), see the diamond data points) is due to the associated reduction in bandgap (see Table 1), which lowers the potential barrier at the doped-source/intrinsic-gated-region interface, thereby improving the transconductance.

Most simulations are performed with an essentially zero-thickness gate electrode. This is convenient from a numerical analysis point-of-view; it reduces the simulation space required to contain source and drain contacts that are sufficiently long to ensure charge neutrality at their ends [33]. However, it is an unrealistic situation, which is also impractical from the point-of-view of obtaining a high f_{max} [30]. Fig. 5 (square data points) shows the effect of increasing the gate-metal thickness from 0.1 nm through 1 to 10 nm. Even though the last value may still be low for a practical device, it does indicate the deleterious effect of the associated increase in C_{Ge}. If a finite contact resistance is added to this, f_T is further reduced: Fig. 5 (cross data points) shows the effect of 5 and 50 kΩ of resistance in the source and drain contacts. The latter may not be unreasonable for nanoscale contacts, and it would

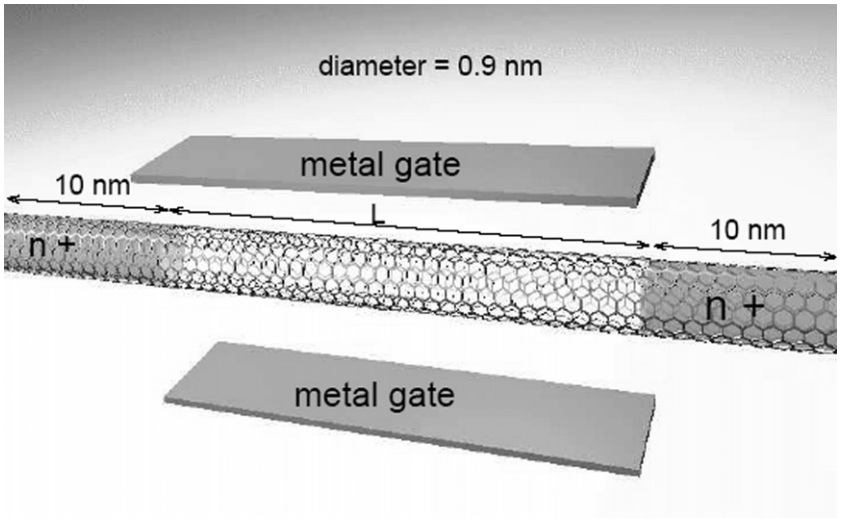

Fig. 4. Doped-contact CNFET with double-gate [3,4].

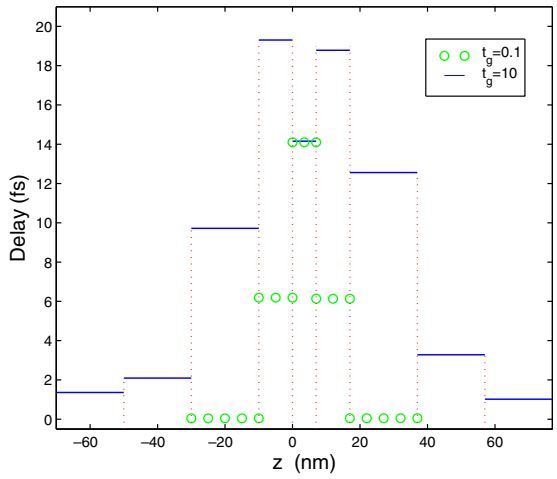

Fig. 6. Regional signal delay for doped-contact n–i–n CNFETs with gate-metal thicknesses of either 0.1 or 10 nm. In each case the gate is centrally located and L_G = 7 nm. Other common parameters are: chirality (11,0), oxide thickness = 2 nm, and source and drain contacts = 70 nm.

bring the estimated value of f_T down to levels that have actually been realized in another type of transistor [13].

The importance of the gate-metal thickness is emphasized in Fig. 6, which breaks down the overall source-drain signal delay τ_{SD} into regional delays [8]

$$\tau_{SD} = \sum_{r}^{L_{CNQ}} \tau_r = \frac{1}{\partial I} \sum_{r}^{L_{CNQ}} \int_r \partial Q(z)\, dz, \tag{3}$$

where L_{CNQ} is the length of the nanotube over which there is a change in charge, $\partial Q(z)$ is the change in local charge density integrated over energy, and ∂I is the change in drain current. Fig. 6 indicates how L_{CNQ} is much enlarged by increasing the gate-metal thickness.

3.3. Comparison of doped-contact- and SB-CNFETs

Figs. 3 and 5 display, to the best of our knowledge, all the simulation results that have been reported thus far for f_T in CNFETs. However, a comparison between SB- and doped-contact-devices is not easily made from this collection because of the differing device properties that have been used, e.g. device chirality, oxide thickness, voltage bias, and because of the different simulators that have been employed. To provide a meaningful comparison, we provide Fig. 7 and Table 2, which compare the salient high-frequency parameters for the two types of CNFET with common parameters of: chirality (19,0), L_G = 7 nm, gate-metal thickness = 5 nm, oxide thickness = 2 nm, source/drain underlap = 5 nm, contact lengths = 45 nm, $|V_{GS}|$ = 0.6 V, $|V_{DS}|$ = 0.7 V. The SB-CNFET used Pd contacts, whereas the doping density in the doped-contact case was 5×10^8/m. The parameter values were chosen in accordance with realizing good high-frequency performance. Note that different parameter values would be needed for a CNFET more suited to high-speed digital-logic applications [34,35], in particular: higher bandgap to produce a reasonable ON/OFF-current ratio, and a longer gate length to reduce source-drain tunneling.

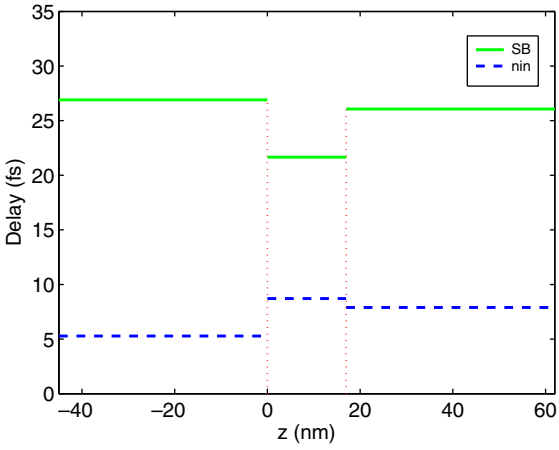

Fig. 7. Comparison of regional signal delays for SB- and doped-contact-CNFETs with properties described in the text.

Table 2
Comparison of small-signal parameters of SB- and doped-contact-CNFETs having the properties listed in the text

Contacts	g_m (μS)	C_{GG} (aF)	f_T (THz)	g_{ds} (μS)	C_{GD} (aF)	R_c (kΩ)	"Extrinsic" f_T (THz)
Pd	19.6	1.47	2.1	1.80	0.66	50	1.0
C (*n*-type)	59.5	1.37	6.9	0.97	0.54	50	2.0

C_{GG} is the total gate capacitance, C_{GD} is the gate capacitance due to a change in V_{DS}, g_{ds} is the drain conductance, R_c is the resistance of each of the source and drain contacts. The extrinsic f_T is computed from Ref. [30].

The Table highlights the significant difference in transconductance between the two devices; this is due to the reduced quantum-mechanical reflection of electrons at the injecting source/intrinsic-nanotube interface. The capacitances are only slightly higher in the SB case, but, when taken together with the lower current, of which the lower g_m is a manifestation, they result in significantly higher regional signal delays, as Fig. 7 shows.

4. Discussion

All of the data presented in this review now falls below the "ultimate" propagation limit [6]. This should now remove speculation about how extraordinarily high values of f_T might arise in nanoscale FETs due to fortuitous variations in local charge densities [1,8]. The possibility of the propagation velocity in regions of high field, such as can exist in the channel of short FETs, being exceeded by the signal velocity has also been ruled out [7]. Essentially, this is because any local changes in charge in the nanotube are imaged on the gate electrode, thereby contributing wholly to the change in input charge. The near one-to-one correspondence of nanotube charge and gate charge arises because of the two-dimensional geometry and the close proximity of the gate electrode to the nanotube. In a bipolar transistor, which is essentially a one-dimensional device, the electrostatics is much simpler, and it is easily shown that not all of the charge change within the semiconducting regions is imaged on the input electrode (the base) [36]. This can lead to the signal delay in the base-collector space-charge region being less than the propagation delay in that region.

Inevitably, when considering the performance of a new field-effect transistor, comparisons will be made with Si MOSFETs. This review has suggested that the signal delay in the non-neutral regions of FETs is unlikely to be less than the band-limited propagation delay. Thus, a relevant question is: how does the band-limited propagation velocity v_{band} for carbon nanotubes compare with that in nanoscale Si structures? The result quoted in Table 1 suggests that carbon nanotubes have a slight advantage as regards the maximum value of v_{band}, at least when compared to the particular Si nanowire cited. Guo et al. have suggested that v_{band} for an ultra-thin body Si MOSFET is about 50% of that in a CNFET [24]. Thus, the ultimate f_T in CNFETs would appear to be only slightly greater than might be achievable with nanoscale Si FETs.

These comparisons are for ballistic transport, and it may be argued that attainment of ballistic transport is more likely in a CNFET than in a Si MOSFET, primarily because of the relatively long mean-free-path associated with phonon scattering in carbon nanotubes, but also because of the more one-dimensional form of a tube, as opposed to that of a wire or a ribbon. However, it seems unreasonable to ignore the effect of surface scattering, which greatly affects the mobility in present Si MOSFETs. The nature of the oxide/semiconductor interface is different in the two devices, of course, but some penetration of the electron wavefunctions into the oxide of a CNFET is to be expected. There is presently no information on this, to the authors' knowledge.

We have shown that when the practical features of gate-metal thickness and contact resistance are included in the simulations, then f_T for CNFETs can drop into the region of 700–800 GHz. This is about a factor of 2 higher than values that have actually been realized already in planar Si MOSFETs [12]. Add this fact to the need to arrange CNFETs in parallel to improve the current drive, and one wonders whether the small material superiority of v_{band} and the geometrical superiorities of a wrap-around gate and a one-dimensional structure, will be enough to combat the matchless technological superiority of silicon FET processing. Perhaps further research and development in high-frequency CNFETs should be directed towards biological applications, for which silicon-based electronics may be less compatible?

5. Conclusions

From this review of the high-frequency performance of CNFETs it can be concluded that:

- experimental f_T values should improve by employing multiple, parallel nanotubes of shorter length than used hitherto;
- theoretically, the effects on f_T of nanotube chirality (diameter), oxide permittivity, gate-source and gate-drain underlap, source- and drain-electrode diameter and resistance, gate-metal thickness, and phonon scattering are well understood;
- doped-contact CNFETs offer better performance capability than Schottky-barrier devices because of their superior transconductance;
- the presently available simulation data indicates that the signal delay time is not less than the propagation time. This suggests that the band-structure-determined velocity is a key factor in assessing the high-frequency prospects for a FET material. The slight advantage that a carbon nanotube has over silicon in this regard may not be sufficient to offset the technological superiority of Si FETs when it comes to processing practical devices.

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References

[1] Pulfrey DL. Critique of high-frequency performance of carbon nanotube FETs. Proc IEEE ESSDERC 2007:234–8.
[2] Le Louarn A, Kapche F, Bethoux J-M, Happy H, Dambrine G, Derycke V, et al. Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors. Appl Phys Lett 2007;90:233108.
[3] Fiori G, Iannaccone G, Klimeck G. Performance of carbon nanotube field-effect transistors with doped source and drain extensions and arbitrary geometry. IEDM Tech Digest 2005:522–5.
[4] Fiori G, Iannaccone G, Klimeck G. A three-dimensional simulation study of the performance of carbon nanotube field-effect transistors with doped reservoirs and realistic geometry. IEEE Trans Electr Dev 2006;53:1782–8.
[5] Fiori G. Private communication; August 29, 2007.
[6] Hasan S, Salahuddin S, Vaidyanathan M, Alam MA. High-frequency performance projections for ballistic carbon-nanotube transistors. IEEE Trans Nanotechnol 2006;5:14–22.
[7] John DL. Limits to the signal delay in ballistic, nanoscale transistors: semiclassical and quantum results. IEEE Trans Nanotechnol 2008;7:48–55.
[8] Pulfrey DL, Castro LC, John DL, Vaidyanathan M. Regional signal-delay analysis applied to high-frequency carbon nanotube FETs. IEEE Trans Nanotechnol 2007;6:711–7.
[9] Kim S, Choi T-Y, Rabieirad L, Jeon J-H, Shim M, Mohammadi S. A poly-Si gate carbon nanotube field-effect transistor for high-frequency applications. In: Proceedings of the IEEE MTT Symposium; 2005. p. 303–6.
[10] Bethoux J-M, Happy H, Dambrine G, Derycke V, Goffman M, Bourgoin J-P. An 8-GHz f_T carbon nanotube field-effect transistor for gigahertz range applications. IEEE Electron Dev Lett 2006;27:681–3.
[11] Narita K, Hongo H, Ishida M, Nihey F. High-frequency performance of multiple-channel carbon nanotube transistors. Phys Status Solidi A 2007;204:1808–13.
[12] Lee S, Jagannathan, Csutak S, Pekarik J, Zamdmer N, et al. Record RF performance of sub-46 nm NFETs in microprocessor SOI CMOS technologies. IEDM Tech Digest 2005:241–4.
[13] Hafez W, Snodgrass W, Feng M. 12.5 nm base pseudomorphic heterojunction bipolar transistors achieving f_T = 710 GHz and f_{max} = 340 GHz. Appl Phys Lett 2005;87:252109.
[14] Wang J, Rahman A, Ghosh A, Klimeck G, Lundstrom M. Performance evaluation of ballistic silicon nanowire transistors with atomic-basis dispersion relations. Appl Phys Lett 2005;86:093113.
[15] Persson MP, Xu HQ. Electronic structure of [1 0 0]-oriented free-standing InAs and InP nanowires with square and rectangular cross-sections. Phys Rev B 2006;73:125346.
[16] Burke PJ. AC performance of nanoelectronics: towards a ballistic THz nanotube transistor. Solid State Electron 2004;48:1981–6.
[17] Castro LC, John DL, Pulfrey DL, Pourfath M, Gehring A, Kosina H. Method for predicting f_T for carbon nanotube FETs. IEEE Trans Nanotechnol 2005;4:699–704.
[18] Koswatta SO, Neophytou N, Kienle D, Fiori G, Lundstrom MS. Dependence of DC characteristics of CNT MOSFETs on bandstructure models. IEEE Trans Nanotechnol 2006;5:368–72.
[19] McGuire DL, Pulfrey DL. Error analysis of boundary-condition approximations in the modeling of coaxially gated carbon nanotube FETs. Phys. Status Solidi A 2006;203:1111–6.
[20] Alam K, Lake R. Performance of 2 nm gate length carbon nanotube field-effect transistors with source/drain underlaps. Appl Phys Lett 2005;87:073104.
[21] Alam K, Lake R. Dielectric sensitivity of a zero Schottky-barrier, 5 nm gate, carbon nanotube field-effect transistor with source/drain underlaps. J Appl Phys 2006;100:024317.
[22] Castro LC. Unpublished data.
[23] Castro LC, Pulfrey DL, John DL. High-frequency capability of Schottky-barrier carbon nanotube FETs. Solid State Phenom 2007;121–123:693–6.
[24] Guo J, Hasan S, Javey A, Bosman G, Lundstrom M. Assessment of high-frequency performance of carbon nanotube FETs. IEEE Trans Nanotechnol 2005;4:715–21.
[25] Pourfath M, Kosina H, Cheong BH, Park WJ, Selberherr S. Improving DC and AC characteristics of ohmic contact carbon nanotube field-effect transistors. Proc ESSDERC 2005:541–4.
[26] Yoon Y, Ouyang Y, Guo J. Effect of phonon scattering on intrinsic delay and cut off frequency of carbon nanotube FETs. IEEE Trans Electron Dev 2006;53:2467–70.
[27] Javey A, Guo J, Farmer DB, Wong Q, Yenilnez E, Gordon RG, et al. Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays. NanoLetters 2004;4:1319–22.
[28] Paul BC, Fujita S, Okajima M, Lee T. Impact of geometry-dependent parasitic capacitances on the performance of CNFET circuits. IEEE Electron Dev Lett 2006;27:380–2.
[29] Chen Z, Appenzeller J, Knoch J, Lin Y-M, Avouris P. The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. NanoLetters 2005;5:1497–502.
[30] Castro LC, Pulfrey DL. Extrapolated f_{max} for carbon nanotube FETs. Nanotechnology 2006;17:300–4.
[31] John DL, Pulfrey DL, Castro LC, Vaidyanathan M. Terahertz carbon nanotube FETs: feasible or fantastical? In: Proceedings of the 31st WOCSDICE 2007; ISBN: 978-88-6129-088-4.
[32] Chen Li. Unpublished data.
[33] John DL, Pulfrey DL. Issues in the modeling of carbon nanotube FETs: structure, gate thickness and azimuthal asymmetry. J Comput Electron 2007;6:175–8.
[34] Pulfrey DL, John DL, Castro LC. In: Proceedings of the 13th International Workshop on Phys Semiconductor Dev; 2005. p. 7–13.
[35] John DL, Pulfrey DL. Switching-speed calculations for Schottky-barrier carbon nanotube field-effect transistors. J Vac Sci Technol A 2006;24:708–12.
[36] Laux SE, Lee W. Collector signal delay in the presence of velocity overshoot. IEEE Electron Dev Lett 1990;11:174–6.