

Introduction to PCB layout

ELEC391 - Spring 2020

PCB Design support for ELEC391:

Altium 2018, 150 licenses

Talks:

- Jan 21 Introduction to PCB layout
- Mar 16 (TBC) Invited talk: PCB Fabrication

Fabrication deadlines, Mondays:

Feb 3, Feb 10, Feb 17, Feb 24, Mar 2, Mar 9, Mar 16

Support & submission instructions posted [here](#)

Contents

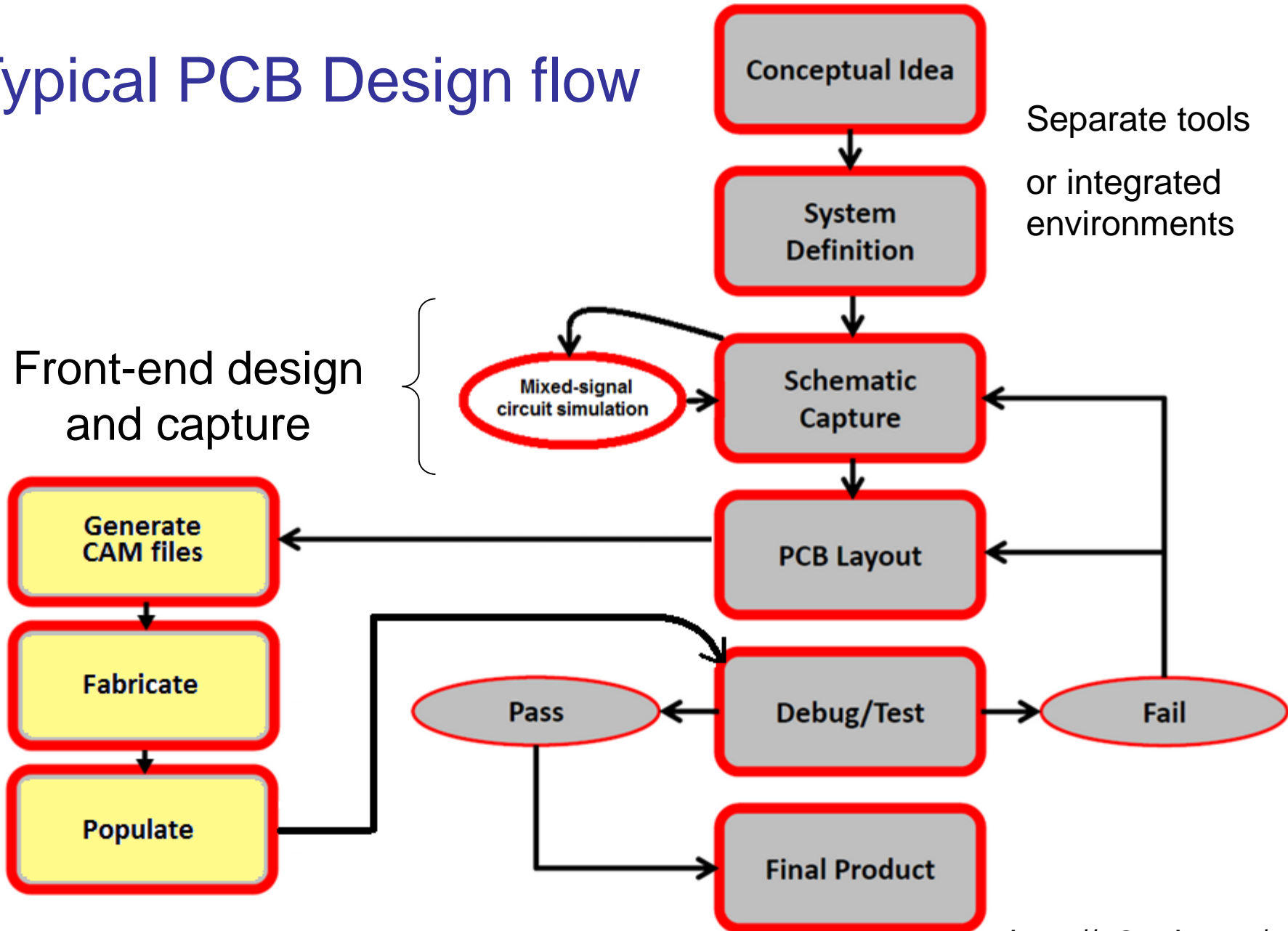
- PCB design flow
- How to install Altium Designer 2018
- Overview of Altium Designer
- Design example as backdrop to introduce PCB concepts
- Instructions for ELEC391 fabrication submissions
- Reference section: PCB design best practices

Credits:

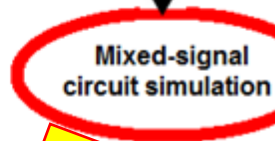
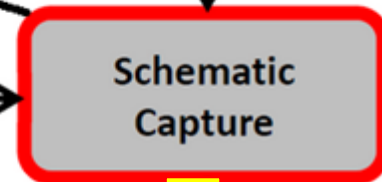
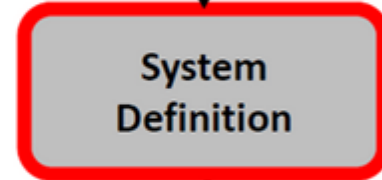
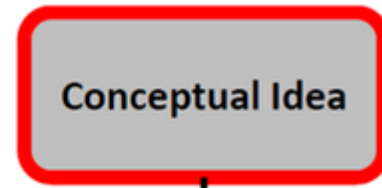
- Unless explicitly stated all source material is from the Altium website and Altium training documents.
- [B1] Complete PCB Design Using OrCad Capture and Layout \ Kraig Mitzner, 2007

PCB Design Flow

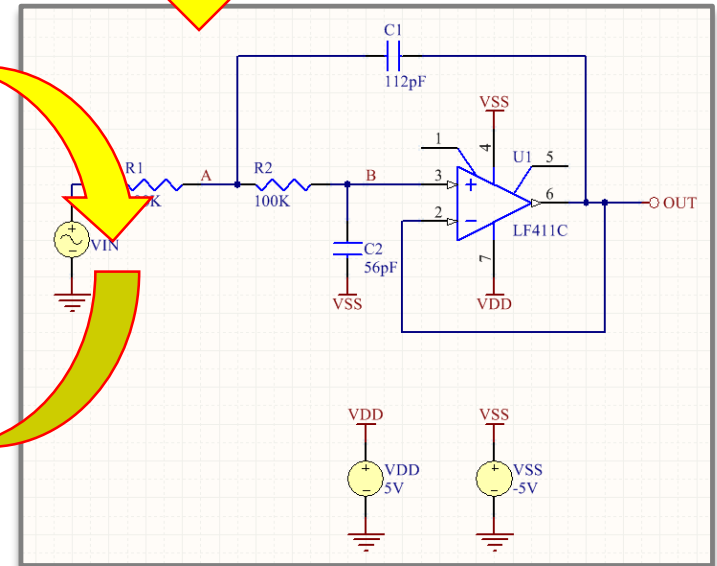
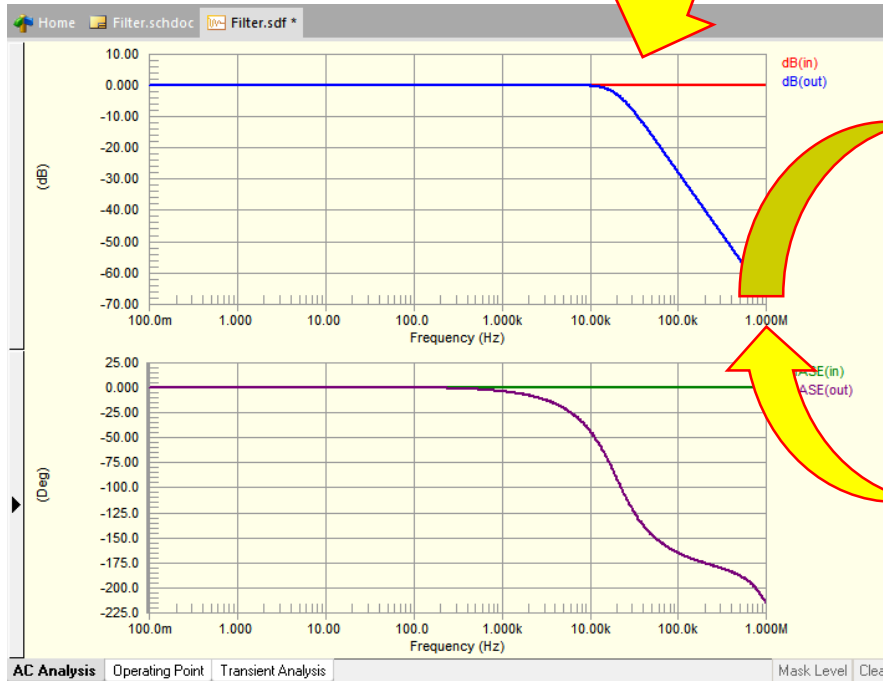
Typical PCB Design flow



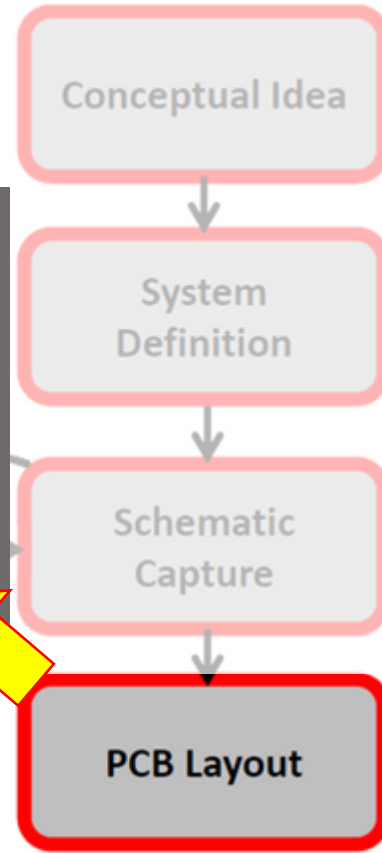
Typical PCB Design flow



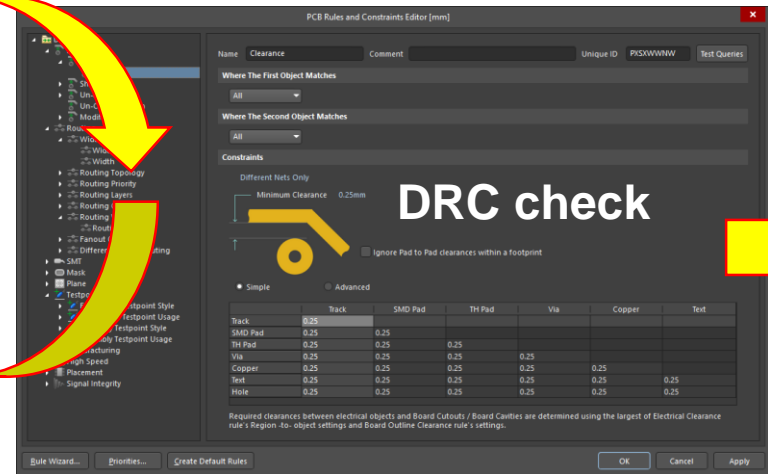
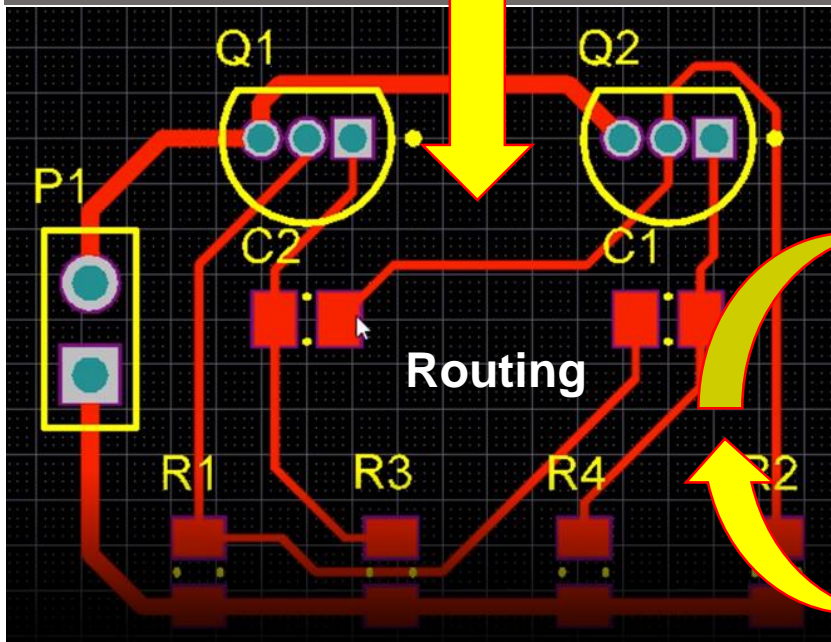
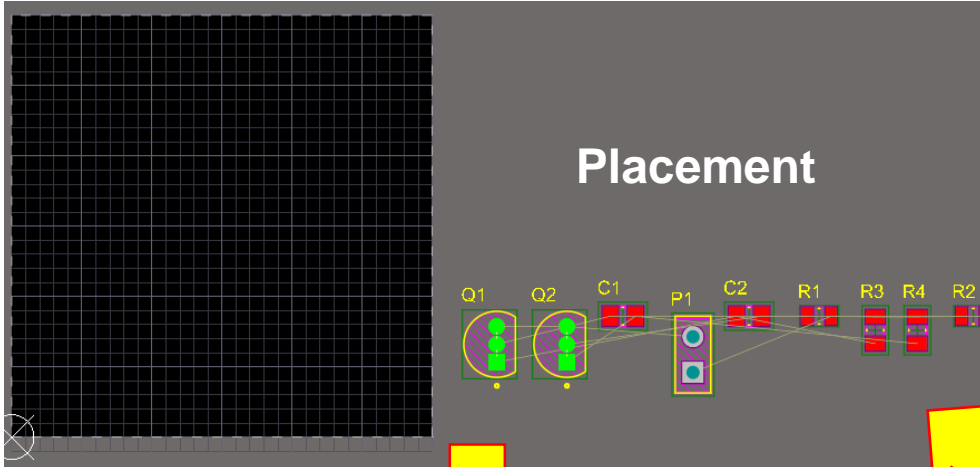
Front-end design and capture



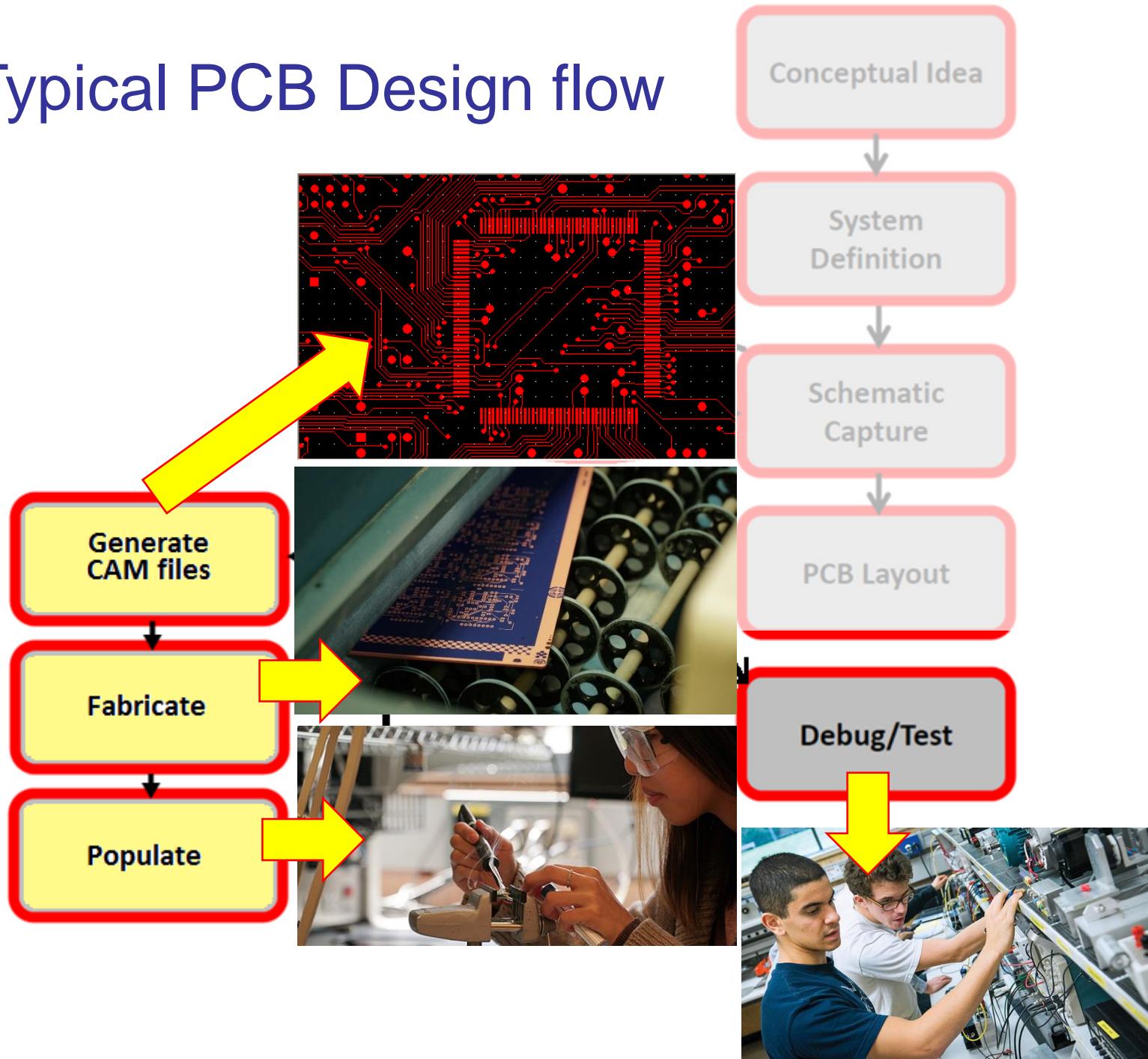
Typical PCB Design flow



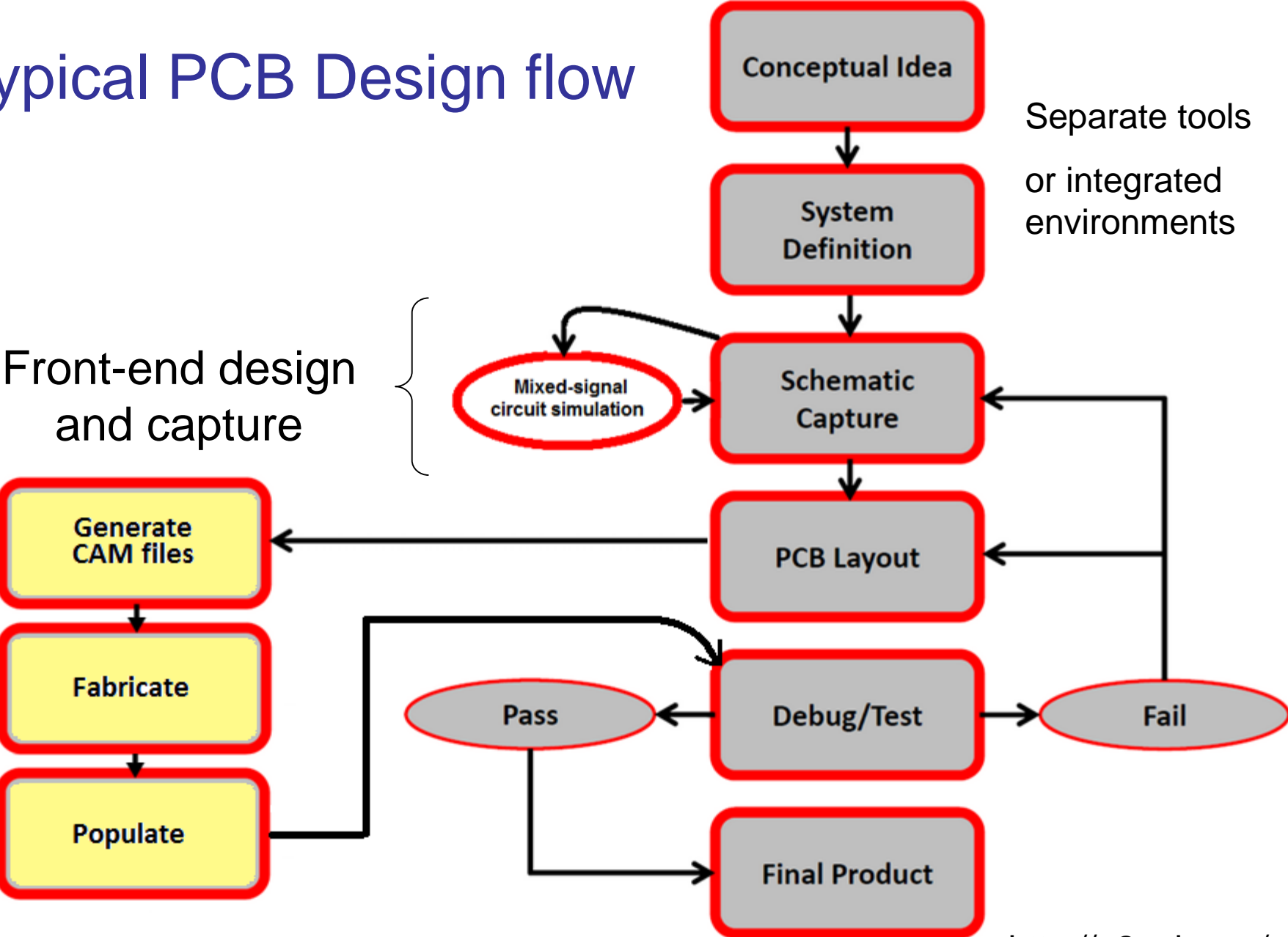
Physical
PCB
Design



Typical PCB Design flow



Typical PCB Design flow



How to install Altium Designer 2018

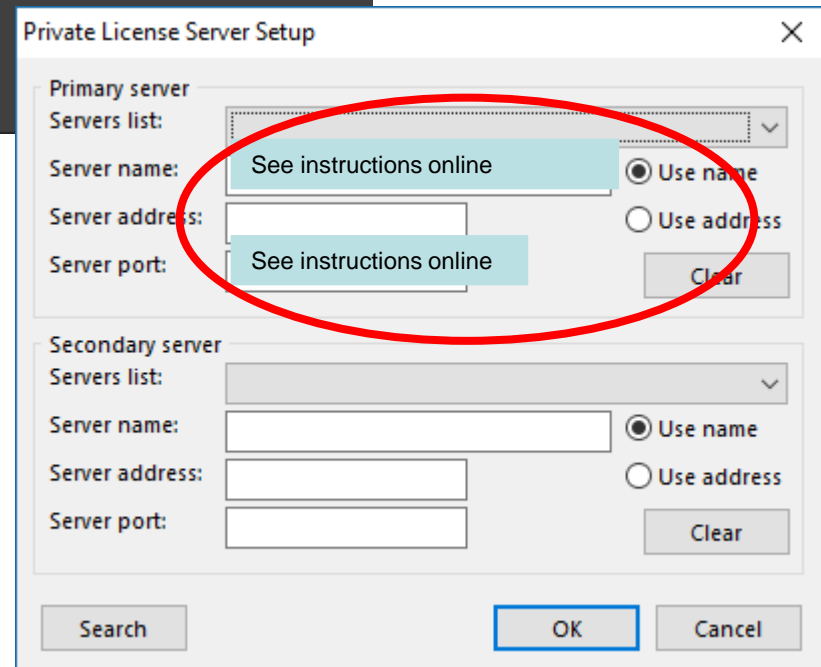
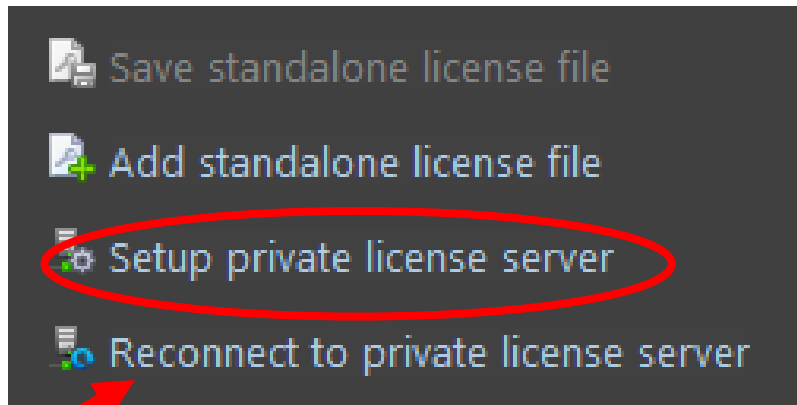
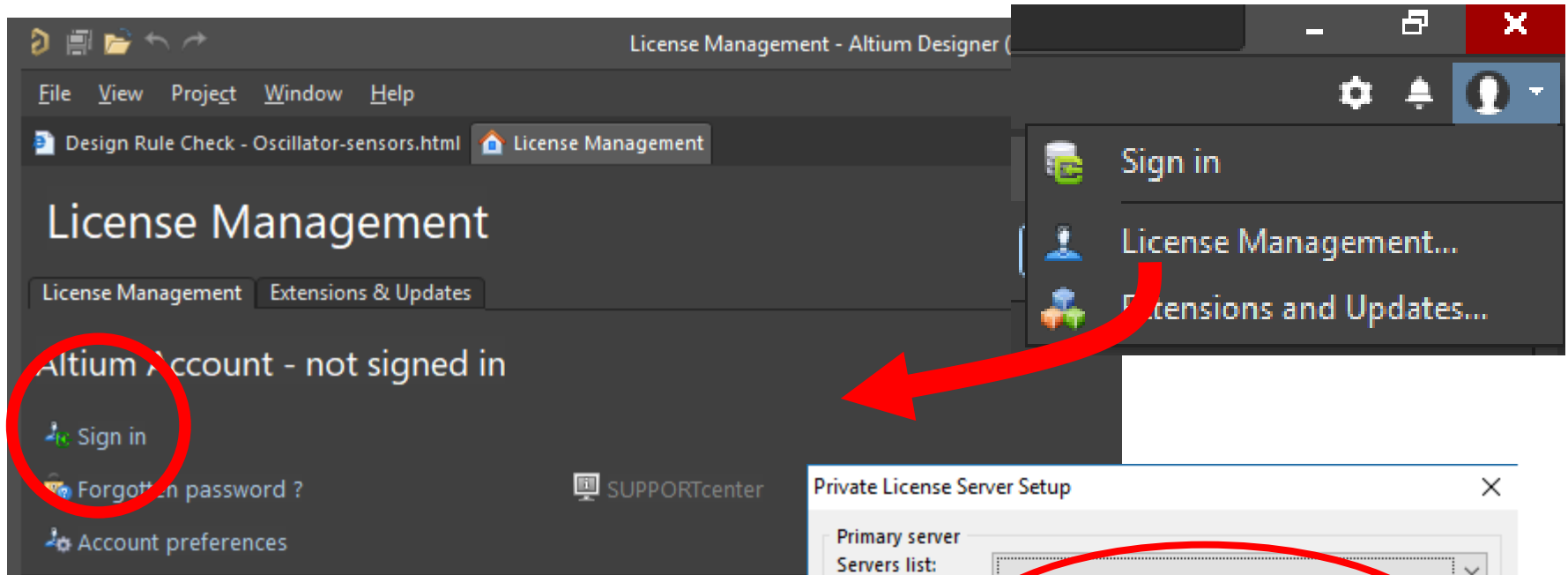
How to install Altium 2018

- Link to instructions:

<https://www.ece.ubc.ca/~eng-services/Altium/>

- Create an account at Altium Live:
email: engservices@ece.ubc.ca (fast)
<http://live.altium.com/#signin> (slow & not linked to our license)
 - Download Altium v2018
 - Connect to license server
- Access to license server:
 - Lab PC or a wired connection to ECE network
 - Wireless connection at UBC (ubcprivate, ubcsecure)
 - My VPN connection

To set the license server



If you loose connection to server click here
If you have problems with server, Disconnect from
& Reconnect to server

To use a license

Right click

Available Licenses - Unlicensed

Warning You are not using a valid license. Select a license below and click Use or Activate.

Product Name	Activation Code	Used	Assigned Seat Count	Expiry	Status	Subscription Status
▶ Altium Designer	7UUP-L42A	-	8/150	16-Oct-2019	OK	Valid to 16-Oct-2019

Use
Roam
Release
Refresh

Warning You are not using a valid license

Private Server - Connected to altium-lm.ece.ubc.ca

Product Name

▶ Altium Designer

Use
Roam
Release
Refresh

4

Release
Refresh
Setup private license server
Disconnect from private license server

If you are having problems with the license server:
Disconnect & Reconnect

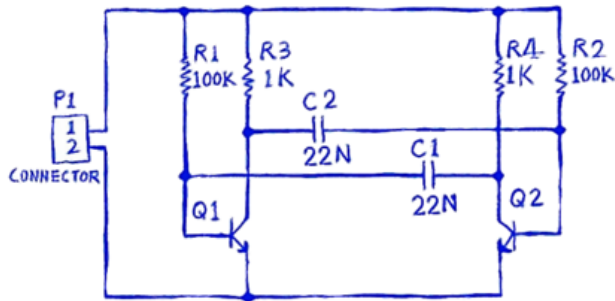
Getting started with Altium Designer 2018

Exploring Altium Designer

Altium Designer documentation:

Do complete this tutorial

Jumping into PCB Design (and Altium Designer)



New to board design? This tutorial shows you where to begin, from creating a schematic to manufacturing a PCB. You'll learn the components you need to get started.

The design you will be capturing and then designing a printed circuit board (PCB) for, is a simple astable multivibrator. The circuit - shown to the left - uses two

general purpose NPN transistors, configured as a self-running astable multivibrator.

The tutorial touches on many of the areas of the software that you will need to become conversant with, in your day-to-day design work - what better way to familiarize yourself with, and get to know, your powerful design 'partner'.

Best training material is on the Altium website. Info is updated, but beware that menus and options change between versions. ver 2018 <> ver 2016

Altium Designer Documentation

18.0

Start Your Free Evaluation

Modified by Jason Howie on Dec 5, 2018

Using Altium Documentation

Altium Designer combines a myriad of features and functionality, including:

- Advanced routing technology
- Support for cutting-edge rigid-flex board design
- Powerful data management tools
- ECAD Libraries containing over 300,000 ready-to-use components
- Powerful design reuse tools
- Real-time cost estimation and tracking
- Dynamic supply chain intelligence
- Native 3D visualizations and clearance checking

ALTUM DESIGNER FREE TRIAL

Overview of Altium Designer

Altium Designer 2018

A unified design environment

[System requirements](#) (MS W7, W8, W10)



- Front-end design and capture
- Physical PCB design
- Mixed-signal circuit simulation
- Signal integrity analysis
- Multi-Board Assembly
- Power Integrity Analyzer
- PCB manufacturing

Professional Design Environment

- Unified platform for individual or corporate use
- Collaborative environment (corporate tool):
 - Multiple users, some with dedicated tasks
 - Design team incremental changes day-by-day
 - Built-in version control (SVN subversion or CVS concurrent versions system)
 - Design repositories / **Vaults** (accessible by multiple users with different credentials)
- Cloud oriented support:
 - Save preferences online
 - <http://live.altium.com/> (forum, design content, blog)
 - Altium Vault (dynamic library of components)

Advice for ELEC391

- Keep it simple
- Focus on schematic entry & layout
- One page schematics
- Locate the right library models for your parts
- Stay away from very small SMD components
- Remember that ECE will take care of CAD file generation and fabrication

Altium Design X2 Environment

The image displays the Altium Design X2 environment with several key components and annotations:

- Top Bar:** Contains the menu bar (File, Edit, View, Project, Place, Design, Tools, Reports, Window, Help) and the "Open documents, and active document" label. The "Preferences and Licensing" button is also visible.
- Project Panel:** Located on the left, it shows a tree view of the project structure, including "Workspace1.DsnWrk", "MiniPC.PrjMbd", and "MiniPC.PrjPcb".
- Editor Active Bar:** A horizontal bar at the top of the workspace containing various tool icons for editing the schematic.
- Pop out panel:** A button in the top right corner used to pop out the Properties panel.
- Properties Floating Panel:** A floating window titled "Properties Floating panel" showing the configuration for a "Power Port" object. It includes a search bar, a "Location" section, and a "Properties" section with fields for "Name" (VDD_DDR), "Style" (Bar), and "Font" (Times New...). It also features bold, italic, and underline formatting buttons.
- Libraries:** A vertical panel on the right side of the workspace.
- Panel access button:** A button in the bottom right corner labeled "Panels".
- Schematic Editor:** The central workspace shows a schematic diagram of a DDR4 memory module. It includes a table of pins and their connections, a network table, and a detailed circuit diagram of the power plane with components like resistors (R221, R223) and capacitors (C282).

Annotations in orange text point to these specific features: "Open documents, and active document", "Editor Active Bar", "Pop out panel", "Properties Floating panel", and "Panel access button".

Recommended basic panels

The screenshot shows the Altium Designer (18.1.6) interface. The main workspace is dark gray. On the left, the 'Projects' panel is visible, showing a tree view of the project structure. On the right, the 'Libraries' panel is open, displaying a list of components and a table of component details. At the bottom, the 'Messages' panel is visible. White text and arrows are overlaid on the image to highlight specific panels:

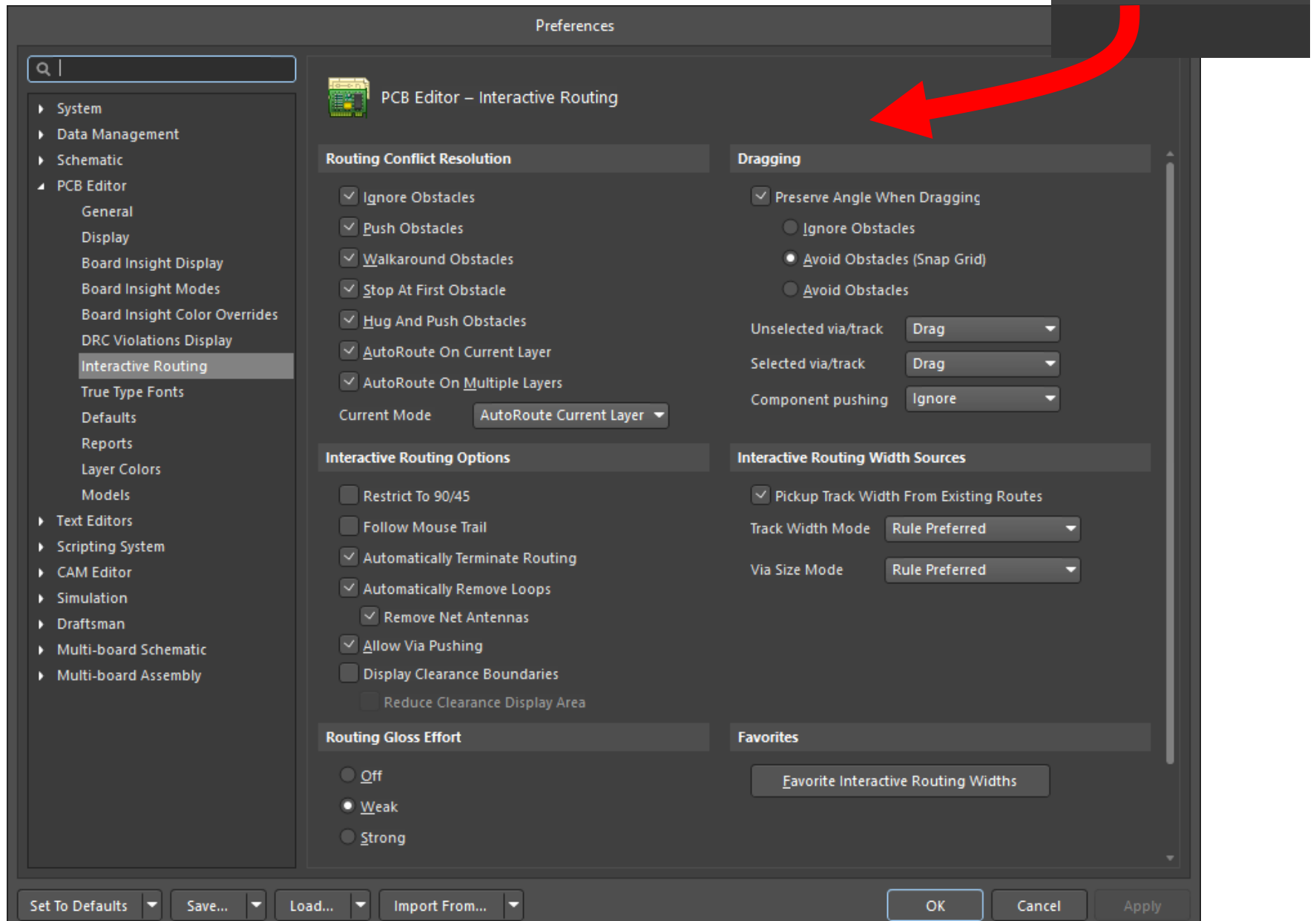
- Libraries & Vault Explorer**: A large white text label with an arrow pointing to the Libraries panel.
- Projects**: A white text label with an arrow pointing to the Projects panel.
- Messages**: A white text label with an arrow pointing to the Messages panel.

The Libraries panel shows the following table:

Model Name	Model Type	Source
2N3904	Signal Integrity	
2N3904	Simulation	2N3904.mdl
TO-92A	Footprint	Miscellaneous Device

For more help working with panels read [this](#)

Preferences Dialog



Tips

(Basics for the single user)



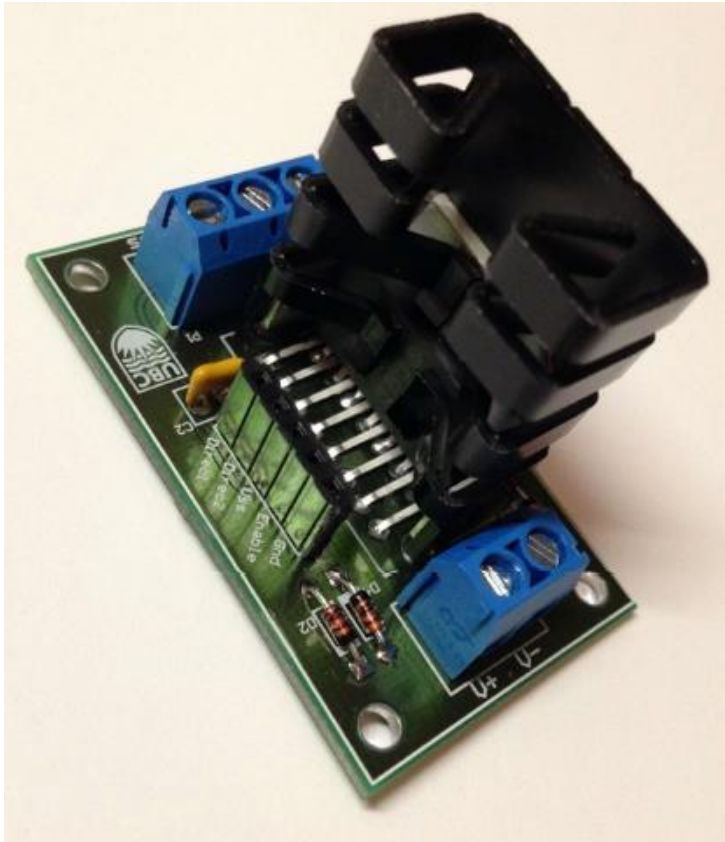
Don't forget:

- Use Keyboard shortcuts
<Shift + F1> while running a command for a list of shortcuts
- <Esc> or Right Click to exit a command mode
- Save documents and project often

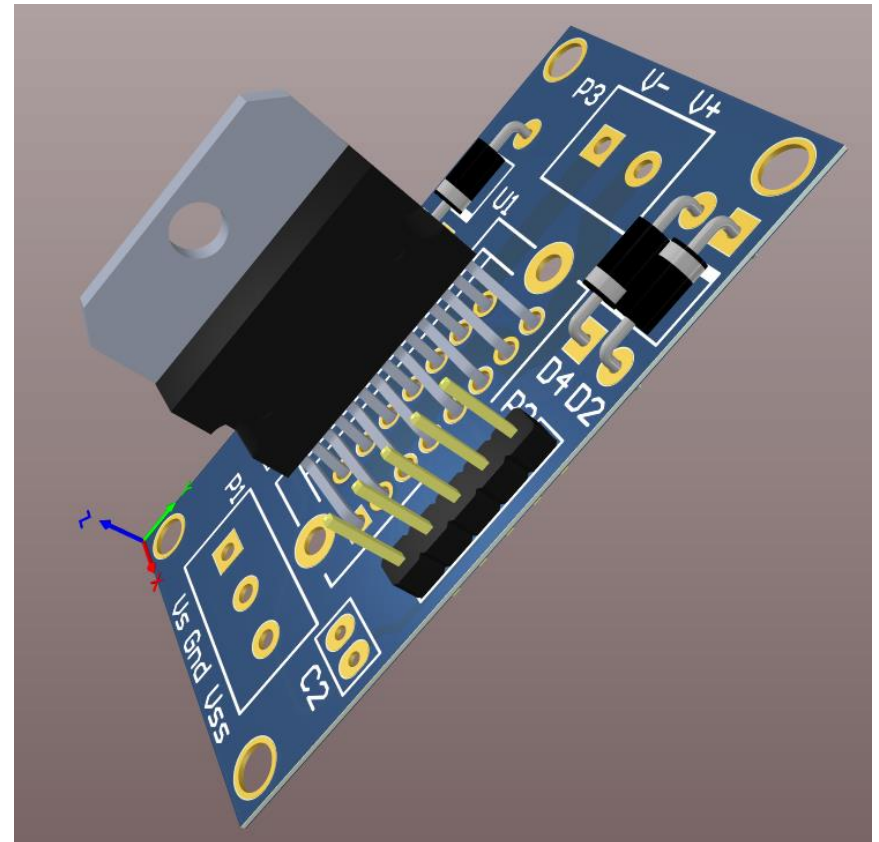
Design Example

Design example

L298 Motor Driver Board
(by Matt Winship)

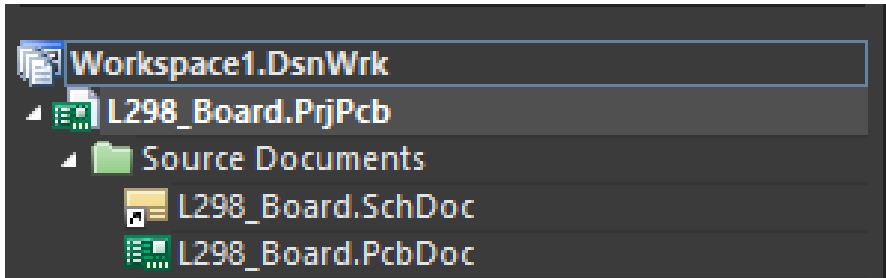


3D View on Layout Editor

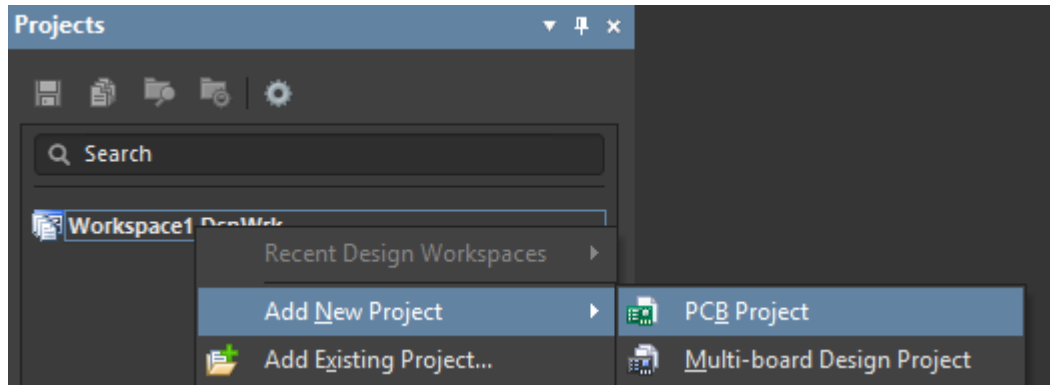


[L298 Motor Driver Board Datasheet.pdf](#)

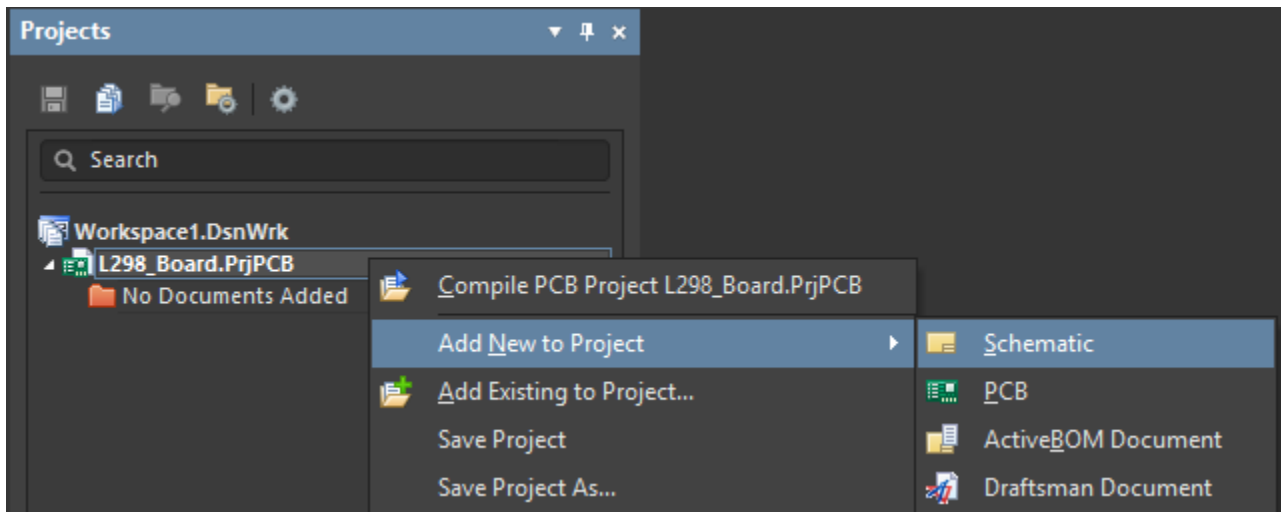
Create project files



1. Project file
2. Schematic file
3. PCB file



When creating the project file remember to use “Save As” to rename. Otherwise your project will be called “PCB_Project1”

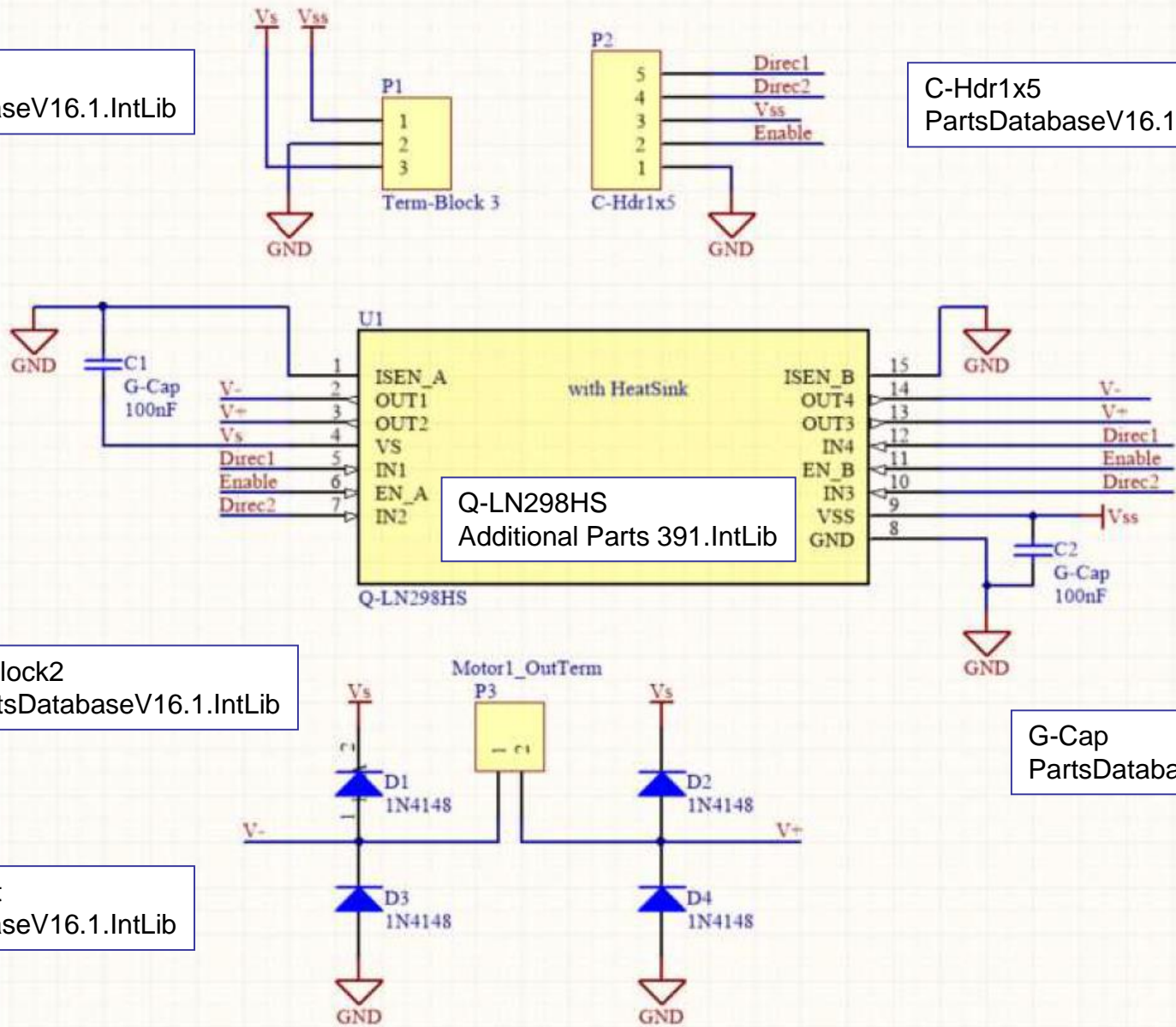


Create Schematic & PCB files. Remember to rename accordingly. It is good practice to save all files in the same directory

L298 Motor Driver Board Schematic

C-Block3
PartsDatabaseV16.1.IntLib

C-Hdr1x5
PartsDatabaseV16.1.IntLib



C-Block2
PartsDatabaseV16.1.IntLib

G-Cap
PartsDatabaseV16.1.IntLib

T-DiodeRect
PartsDatabaseV16.1.IntLib

Steps to create the Schematic

1. Load libraries
2. Draw the schematic
Set electrical type for connector pins
3. Compile Project:
Project → Project Options
[More on: Compiling and Verifying the Design](#)
4. Place no ERC labels if necessary
Modify connection matrix with caution
[More on: No ERC Directive](#)

Wiring Tips

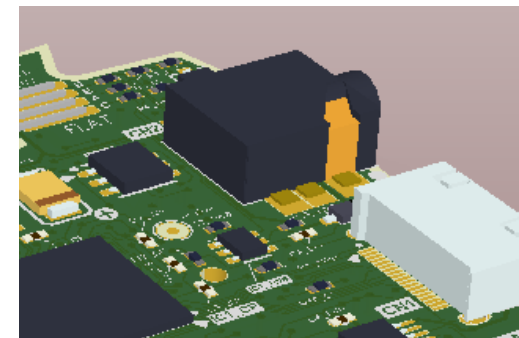
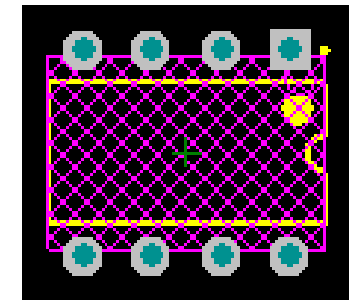
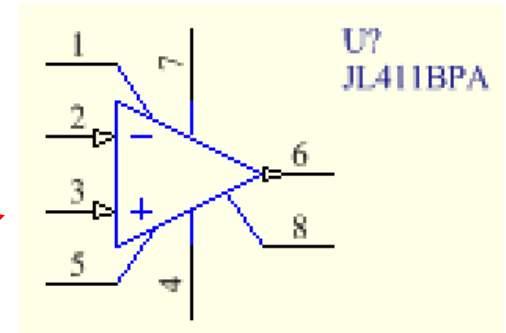
- **Left-click** or **<Enter>** to anchor the wire at the cursor position.
- **<Backspace>** (**←**) to remove the last anchor point.
- **<Spacebar>** to toggle the direction of the corner.
- **<Shift+Spacebar>** to cycle through all possible corner modes.
- **Right-click** or **<Esc>** to exit wire placement mode.
- To graphically edit the shape of a wire, Click once to select it first, then Click and hold on a segment or vertex to move it.
- Whenever a wire crosses the connection point of a component, or is terminated on another wire, a junction will automatically be created.
- A wire that crosses the end of a pin will connect to that pin, even if you delete the junction.
- To move a placed component and drag connected wires with it, hold down the **Ctrl** key while moving the component, or select **Move » Drag**.

About Libraries

[More on: Understanding Models, Components and Libraries](#)

- Component representations for different phases of design:

- Schematic symbol
- PCB footprint
- SPICE model definitions
- Signal integrity description
- 3D graphical description



```
*****INPUT STAGE*****
```

```
*
IOS 2 1 25.0P
*^Input offset current
CI1 1 0 3P
CI2 2 0 3P
R1 1 3 1E12
R2 3 2 1E12
I1 99 4 1.0M
J1 5 2 4 JX
J2 6 7 4 JX
R3 5 50 650
R4 6 50 650
*Fp2=28 MHZ
G1 5 6 4 3700
```

Libraries = collection of components

- Collection of components, models or both
- Model Libraries (*.MDL, *.CKT, *.PCBLib)
 - Simulation models are one file per model
 - PCBLib libraries are typically a collection of footprints
- Schematic Libraries (*.SchLib)
 - Symbol and a link to a model library
- Integrated Libraries (*.IntLib)
 - Symbol, footprint and other models are compiled into a single portable file to create ...
 - Unified components with links to all domain models + parametric information

Obtaining integrated libraries

1. Altium default libraries

Miscellaneous Connectors

Miscellaneous Devices

2. Altium Vault

Cloud dynamic collection of unified components
includes real-time supply chain information

3. Frozen (legacy) libraries: [from here](#)

you can install anywhere but it is a good idea to make a subfolder under:
C:\Users\Public\Public Documents\Altium\AD18\Library
or a cloud storage service if you work from more than one PC

4. AltiumLive website: [Resources / Design Content](#)

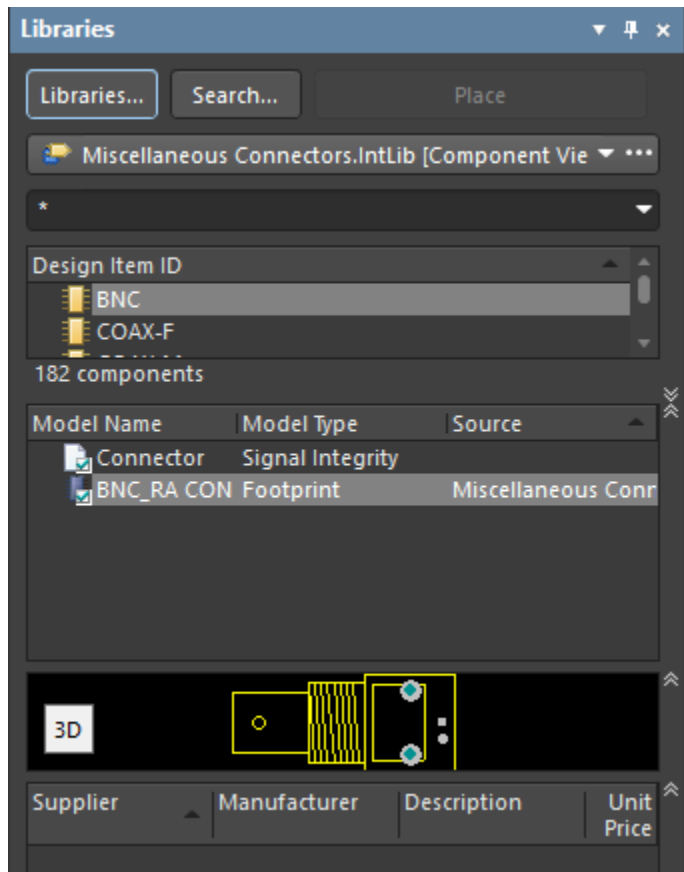
5. IC Manufacturer sites (specially simulation models)

6. ELEC391 libraries from last year: [here](#)

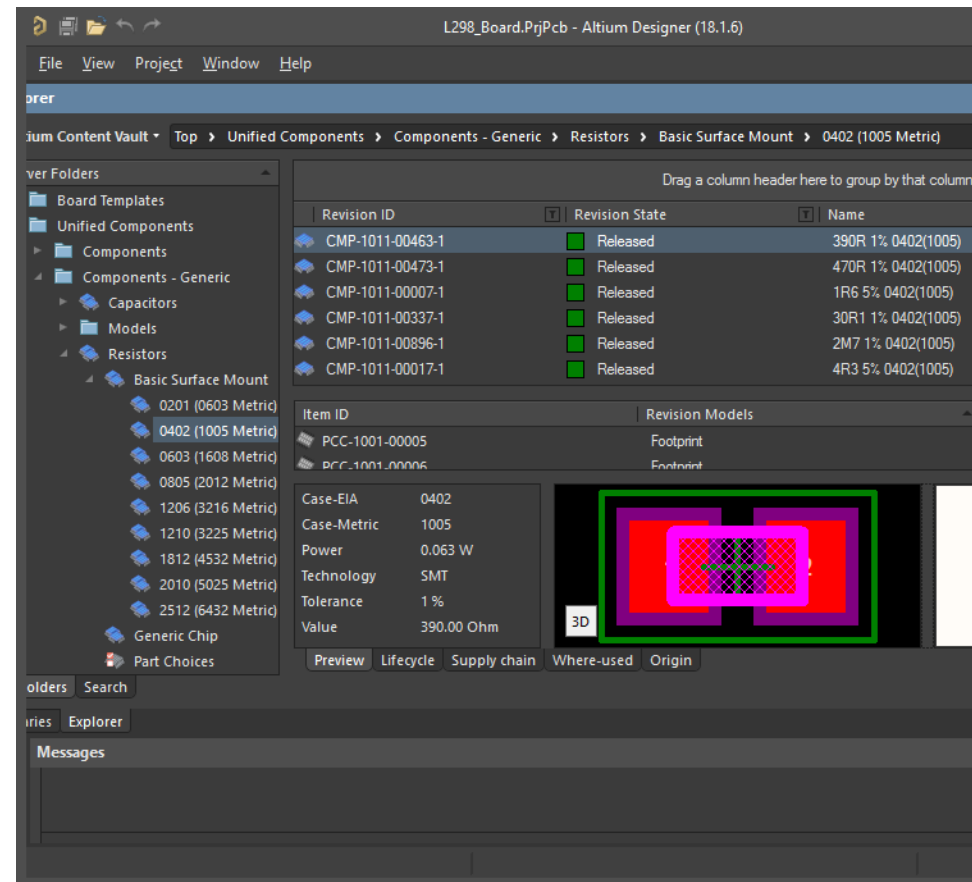
7. Make your own

Accessing libraries

1. Library Panel



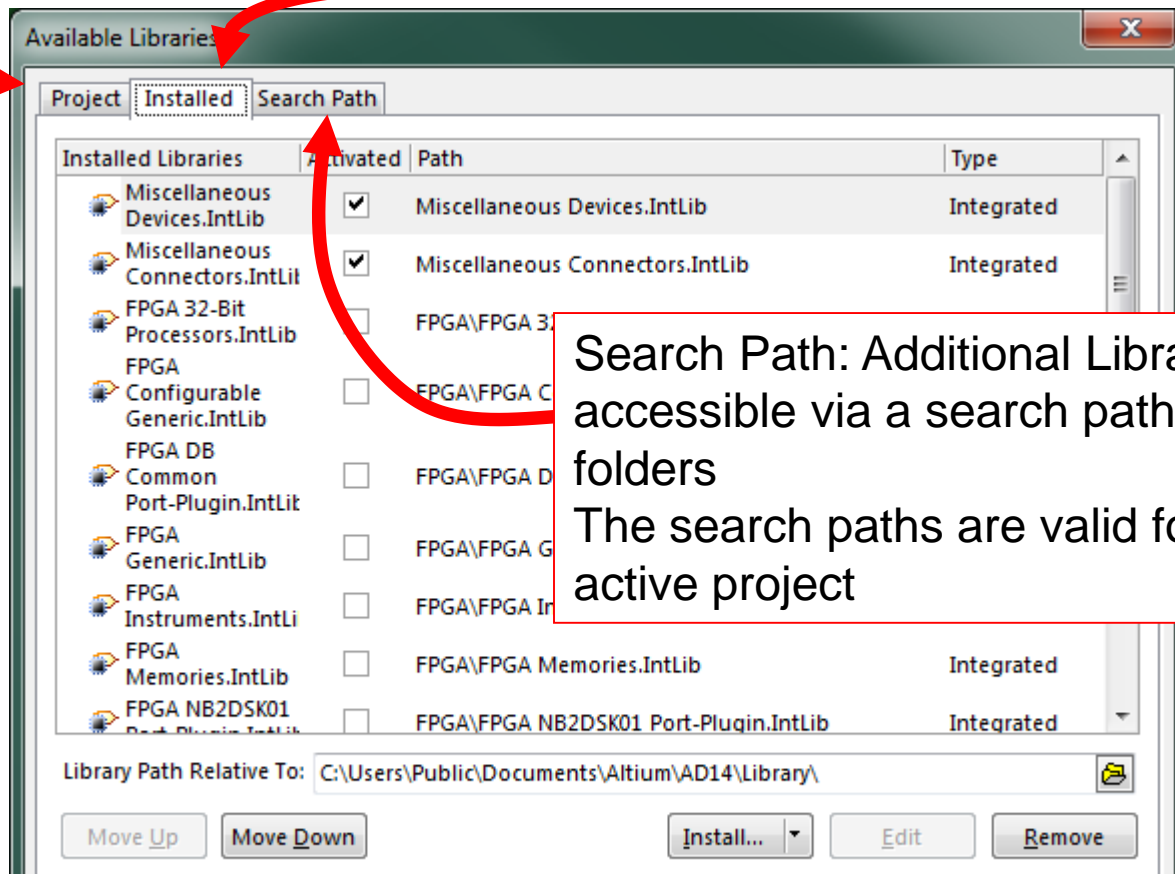
2. Explorer Panel (with an Altium Live account)



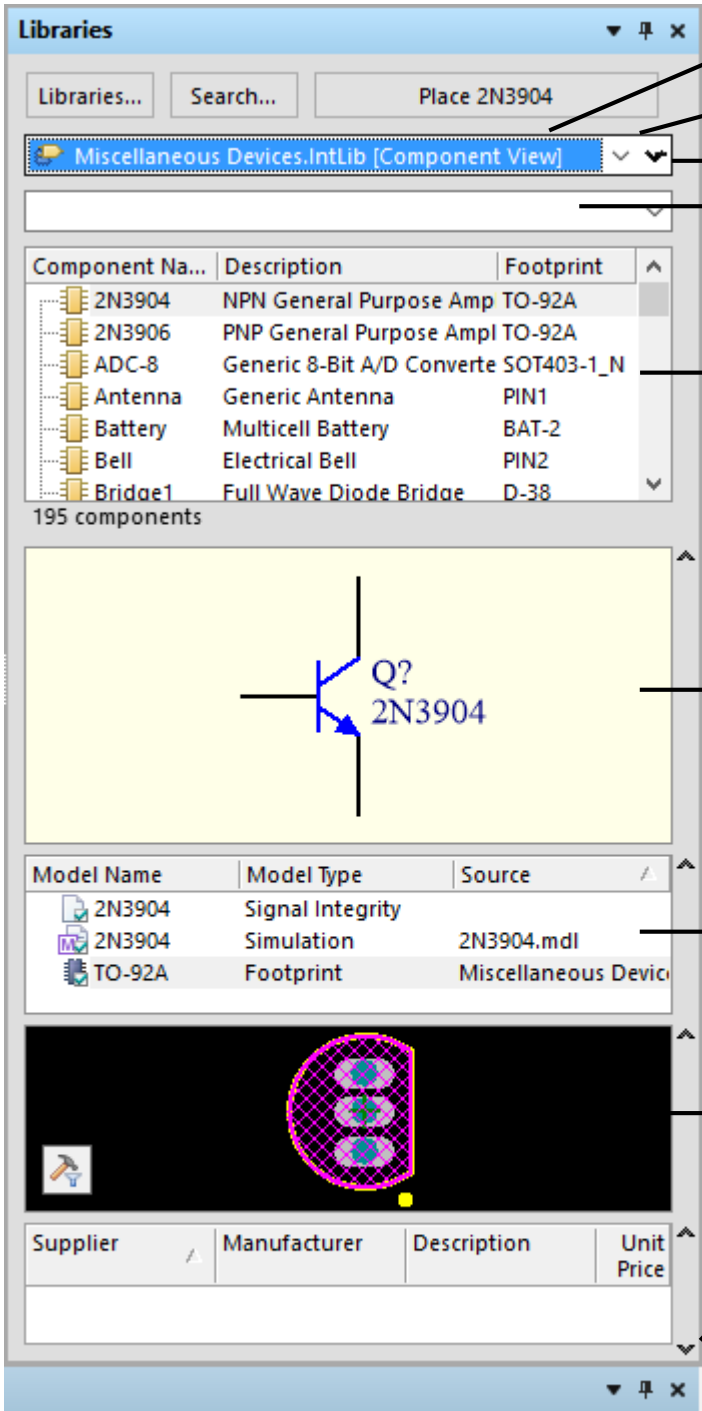
Configuring libraries

Project: part of and available only to the active project and its documents
You have to keep track of where these are if you move the project files

Installed: All installed libraries.
Components are available to all open projects and list is persistent across design sessions



Search Path: Additional Libraries accessible via a search path and sub-folders
The search paths are valid for the active project



Current library

Select a different library

Set library browse mode

Search in current library

List of components.
Select the component of interest

Schematic symbol for selected component

Models linked to the selected component

Graphical display of the selected model

Icons used to show/hide panel sections

Libraries Panel:

All libraries available to the active project

Project + Installed + Search Path

When placing component:

<spacebar> to rotate

<x> or <y> to flip

<Tab> open properties dialog

<L> for PCB footprints to flip component side

To search across libraries:

Search ...

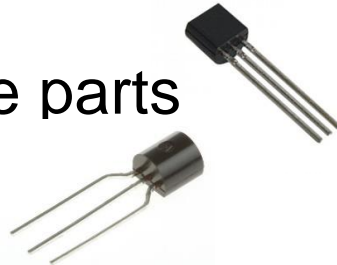
How to select items from the Vault?

Often you will get several choices for the same part, e.g.

Revision ID	Revision State	Name	Description
CMP-1048-01464-1	Released	BC547CG	Amplifier Transistor, NPN Silicon, 3-Pin TO-92, Pb-Free, Bulk Box
CMP-1048-01437-1	Released	BC547C	Amplifier Transistor, NPN Silicon, 3-Pin TO-92, Bulk Box
CMP-1048-01606-1	Released	BC547CZL1G	Amplifier Transistor, NPN Silicon, 3-Pin TO-92, Pb-Free, Ammo Box

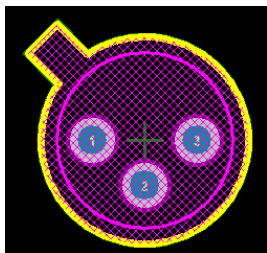
These are typically different component or shipping packaging options. Read the description and check the footprints carefully

Bulk (TO-92) = loose parts
Ammo Box (TO-92)

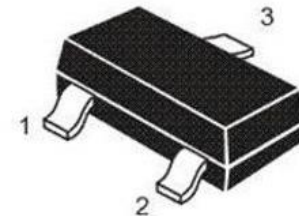
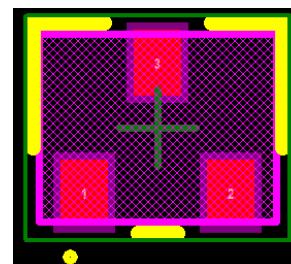


RoHS = Compliance

2N2222 (TO-18)

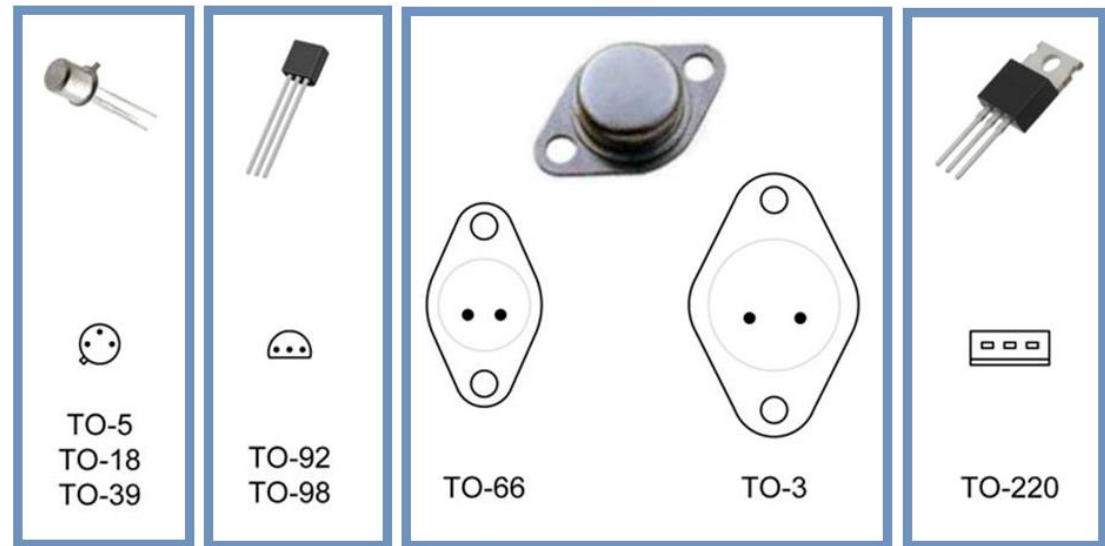
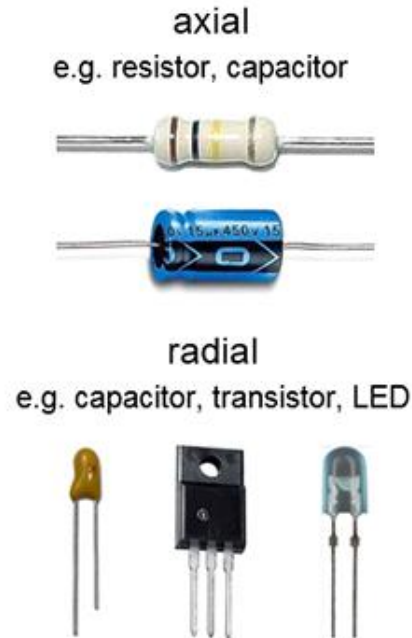


2N2222 (3-Pin SMD)

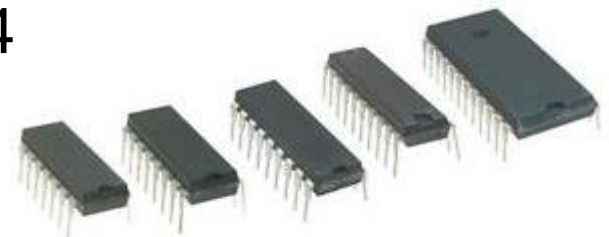


Through-hole Packages & Components

- Use holes drilled through the PCB for mounting the components which are (typ.) soldered on the bottom layer



- Dual in-line package, DIPn → DIP14
Pin spacing is 0.1"
TTL, CMOS, Linear (Analog) ICs



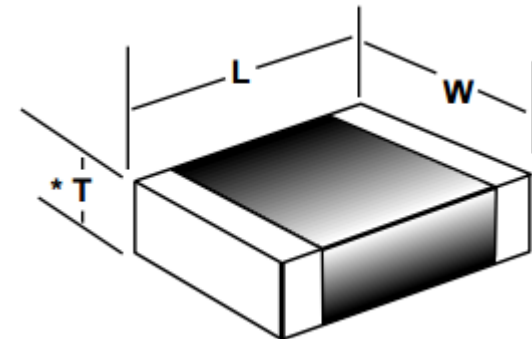
Surface Mount Packages

- Use SMD for high density, small parasitics, or a specific IC
- Passives Flatchip (ceramic Rs, Cs) 4-digit size code

http://www.topline.tv/SMT_Nomenclature.pdf

Size Code		Approximate Size (LxW)	
Inch	Metric	Inch	Metric
0402	1005*	.04" x .02"	1.0 x 0.5mm
0504	1210*	.05" x .04"	1.2 x 1.0mm
0603	1508	.06" x .03"	1.5 x 0.8mm
0805	2012	.08" x .05"	2.0 x 1.2mm
1005*	2512	.10" x .05"	2.5 x 1.2mm
1206	3216	.12" x .06"	3.2 x 1.6mm
1210*	3225	.12" x .10"	3.2 x 2.5mm
1812	4532	.18" x .12"	4.5 x 3.2mm
2225	5664	.22" x .25"	5.6 x 6.4mm

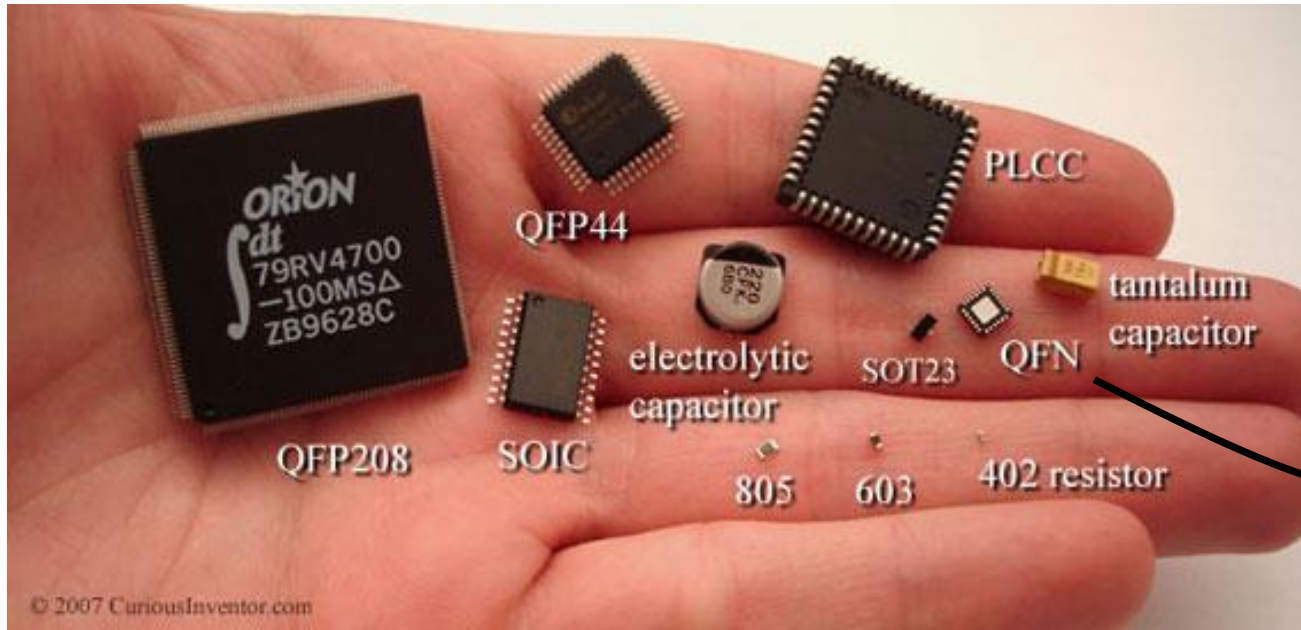
Caution: Overlapping size codes. Metric appears same as inches.



Example:

12	10
Length	Width
.12" or 1.2mm	.10" or 1.0mm

Surface Mount Packages



Difficult to solder by hand

- There are many types of packages (with leads, lead-less)
- [List of integrated circuit packaging types \(wikipedia\)](#)
[List of integrated circuit package dimensions](#)
- Good visual reference is the NXP posters
[Discretes package poster.pdf](#)
[Discrete Flat No-leads DFN package poster.pdf](#)

Footprints are made out of pads

- Pads: contact areas for soldering components, test points, and solder traps
- Pads can have any shape
- Single layer pads: Top/bottom layer, common for SMT, end launch connectors
- Multi-layer pads: for through hole components
- Footprints are a collection of pads

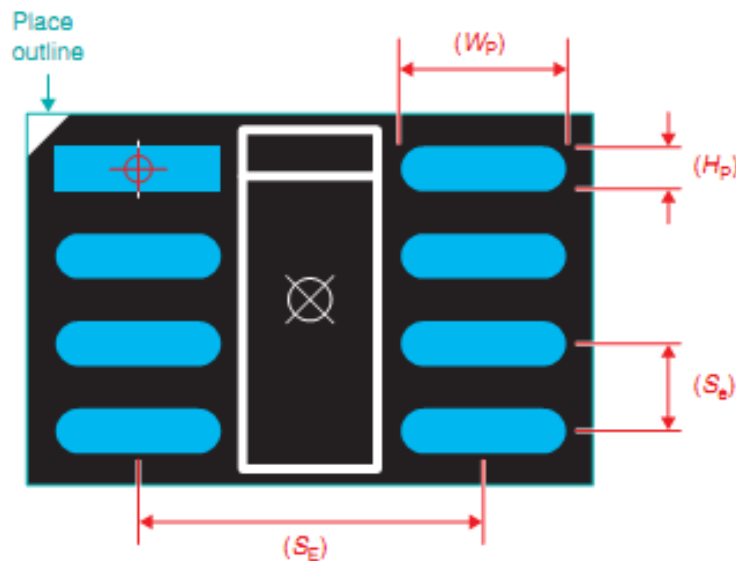


Figure 5-7 Footprint dimensions (typical convention).

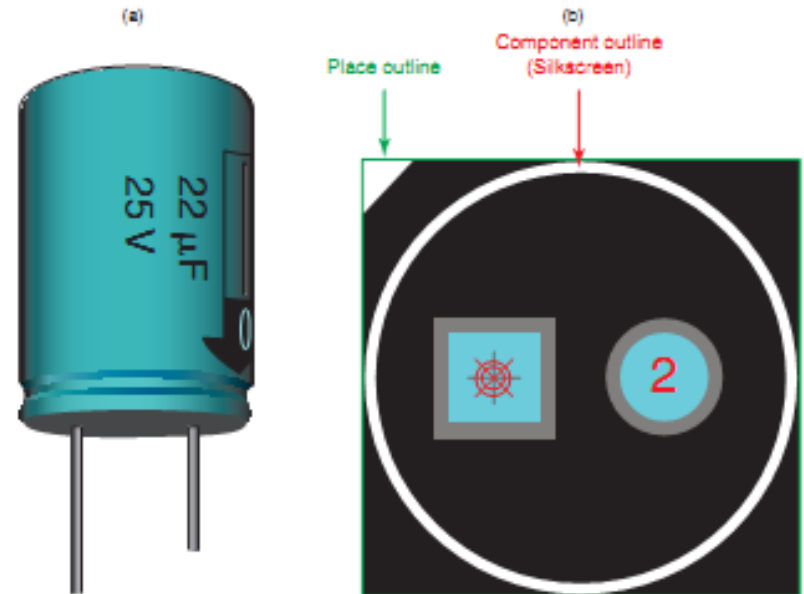
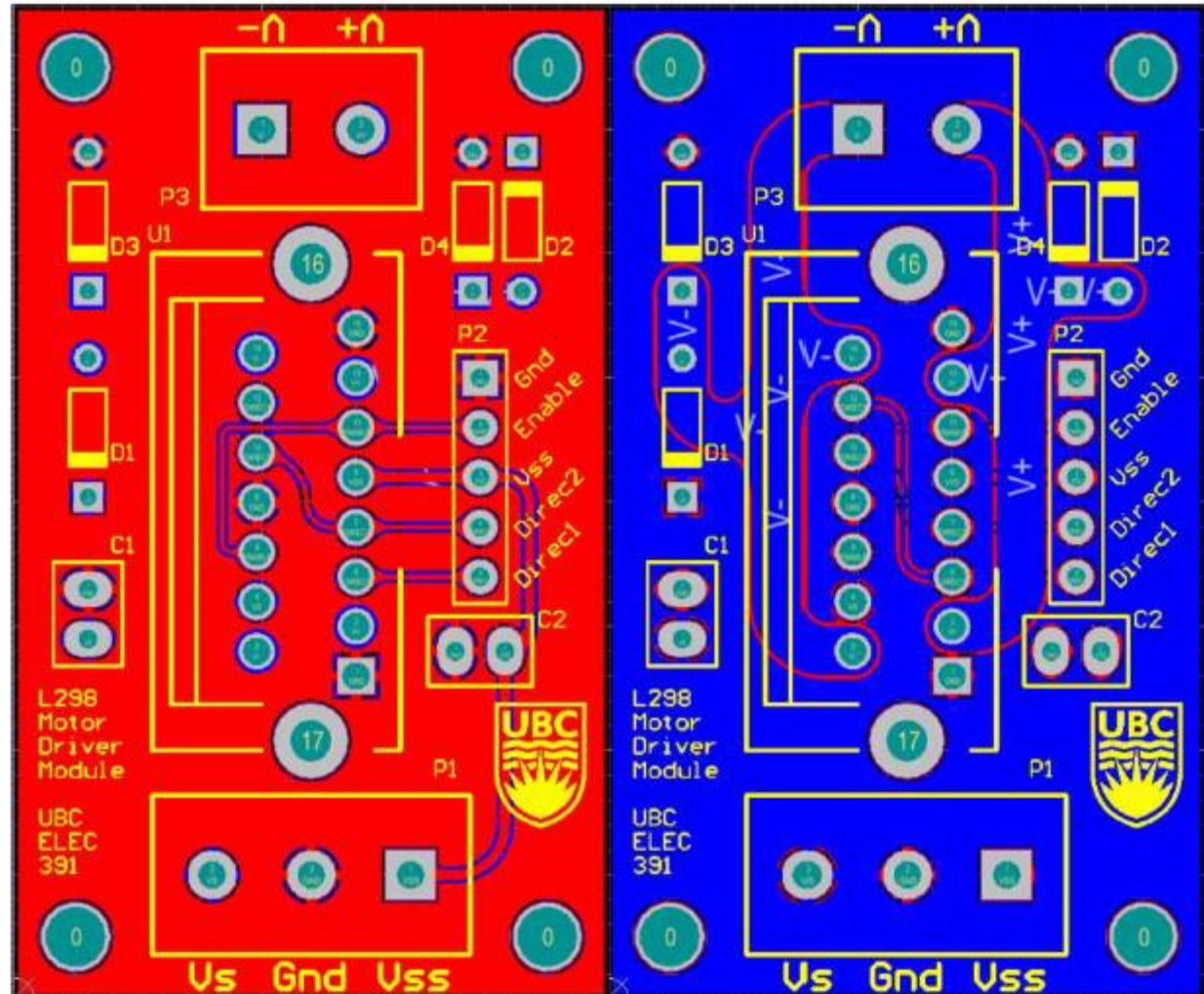


Figure 5-12 Radial-leaded through-hole device. (a) Axial-leaded capacitor. (b) Layout axial footprint

LM298 Motor Driver Board Layout

Board Layout

- Size 1.2" x 2"
- 2 layers
- Mounting holes
- Thick traces for V- and V+
- Power planes for Vs and GND



Top Metal

Bottom Metal

2 starting points for PCB design

1. From a companion schematic package
 - Prepare project schematics
 - Import schematic design
 - Component footprints are added automatically
 - Connectivity is indicated with rats nests
 - Net names are imported from the schematic
2. Directly from the PCB editor
 - You need to select and place manually each component footprint from a library
 - No rats nest – connectivity
 - You must assign nets manually (at least GND)

Steps to complete the Layout

Setup

1. Choose work units (metric or imperial)
you can switch at any time
2. Set the grid
3. Define the board shape
plan for mounting holes and account for connectors
4. Set the origin
although you can move it for convenience as you work



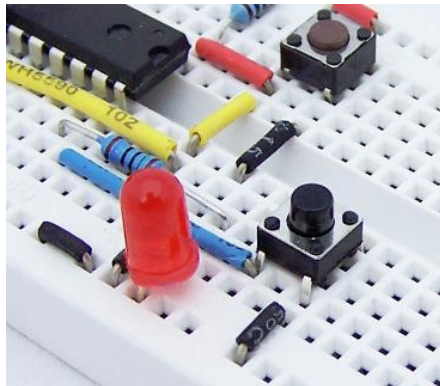
Layout

5. Transfer the design from the schematic
6. Place components and mounting holes
7. Route
8. Draw a board outline, add labels (group #)
9. DRC Check

Working units

- Imperial (inches)

- 1/1000th of an inch = 1 mil = 1thou
- 100mils (0.1”) is a common dimension



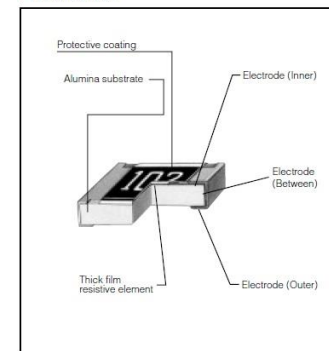
- Metric (mm)

- 1 mm ≠ 1mil !
- Common unit in SM parts

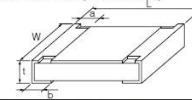
Panasonic

Thick Film Chip Resistors

Construction



Dimensions in mm (not to scale)



Type (inches)	Dimensions (mm)					Mass (Weight) (g/1000 pcs.)
	L	W	a	b	t	
ERJ6S (01005)	0.40 ^{+0.02}	0.20 ^{+0.02}	0.10 ^{+0.02}	0.10 ^{+0.02}	0.13 ^{+0.02}	0.04
ERJ6G (02011)	0.60 ^{+0.03}	0.30 ^{+0.03}	0.10 ^{+0.03}	0.15 ^{+0.03}	0.23 ^{+0.03}	0.15
ERJ6G (0402)	1.00 ^{+0.04}	0.50 ^{+0.04}	0.20 ^{+0.04}	0.25 ^{+0.04}	0.35 ^{+0.04}	0.8
ERJ3G (0603)	1.60 ^{+0.06}	0.80 ^{+0.06}	0.30 ^{+0.06}	0.30 ^{+0.06}	0.45 ^{+0.06}	2
ERJ6G (0805)	2.00 ^{+0.08}	1.25 ^{+0.08}	0.40 ^{+0.08}	0.40 ^{+0.08}	0.60 ^{+0.08}	4
ERJ6G (1206)	3.20 ^{+0.12}	1.60 ^{+0.12}	0.50 ^{+0.12}	0.50 ^{+0.12}	0.60 ^{+0.12}	10
ERJ14 (1210)	3.20 ^{+0.12}	2.50 ^{+0.12}	0.50 ^{+0.12}	0.50 ^{+0.12}	0.60 ^{+0.12}	16
ERJ12 (1812)	4.50 ^{+0.20}	3.20 ^{+0.20}	0.50 ^{+0.20}	0.50 ^{+0.20}	0.60 ^{+0.12}	27
ERJ12Z (2010)	5.00 ^{+0.20}	2.50 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.12}	27
ERJ1T (2512)	6.40 ^{+0.20}	3.20 ^{+0.20}	0.65 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.12}	45

- Remember: 100mils = 2.54mm

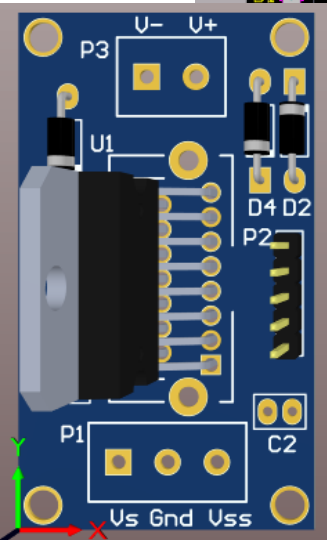
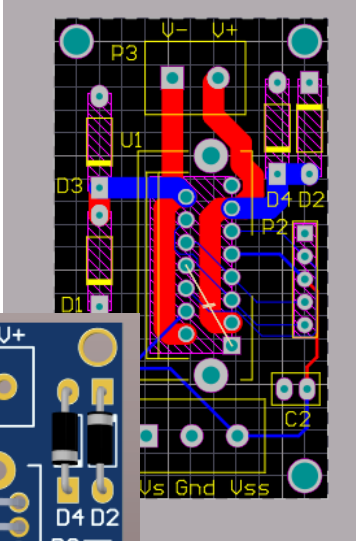
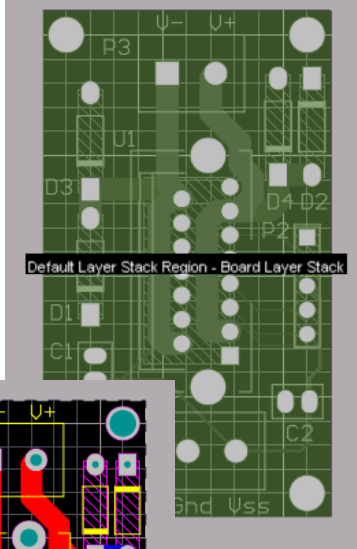
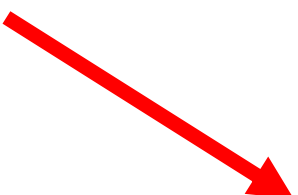
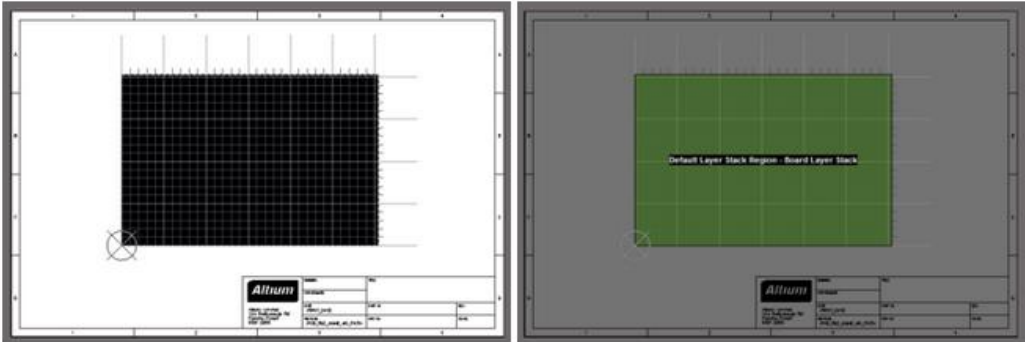
- To switch units in Altium Press <Q>

About the grid ...

- The PCB Editor is a grid based environment
- Objects are placed on a 'placement or snap grid'
- Placement is assisted such as the user doesn't need to aim with absolute accuracy
- Unified Cursor-Snap System >> Properties Panel
 - User defined grids (Cartesian & Polar), that can start at any location and cover different size areas
 - **Default snap grid is called: Global Board Snap Grid**
 - Press <G> to set Global grid step, define grids etc.
- You can work with just the Global Grid, and adjust the step to coarse when placing parts, and fine values when routing
 - More about the PCB Grid system [here](#)

PCB Editor view modes

- Viewing modes:
 - Board Planning Mode <1>
 - Design » Edit Board Shape
 - Design >> Move Board Shape
 - 2D Layout Mode <2>
 - 3D Layout Mode <3>



Design transfer

Design >> Update PCB Document ...

Setup steps

The screenshot shows a PCB design software interface with two tabs at the top: 'L298_Board.SchDoc' and 'L298_Board.PcbDoc'. The main workspace is divided into a grid on the left and a schematic diagram on the right. The schematic diagram, titled 'L298_Board', shows various components connected by lines. Components include resistors (D3, D4, D1, D2), capacitors (C2, C1), an integrated circuit (U1), and connectors (P1, P2, P3). Each component is highlighted with a colored box corresponding to its footprint: resistors are green, capacitors are yellow, the IC is blue, and connectors are purple. A red box highlights the 'L298_Board' component. A text box on the right explains that 'Rat's nests indicate connectivity as per schematic (Net names are assigned to part terminals)'. At the bottom, a legend bar shows color-coded boxes for 'Top Layer', 'Bottom Layer', 'Mechanical 1', 'Top Overlay', 'Bottom Overlay', 'Top Paste', and 'Bot'. The 'Bot' box is partially obscured by a mouse cursor.

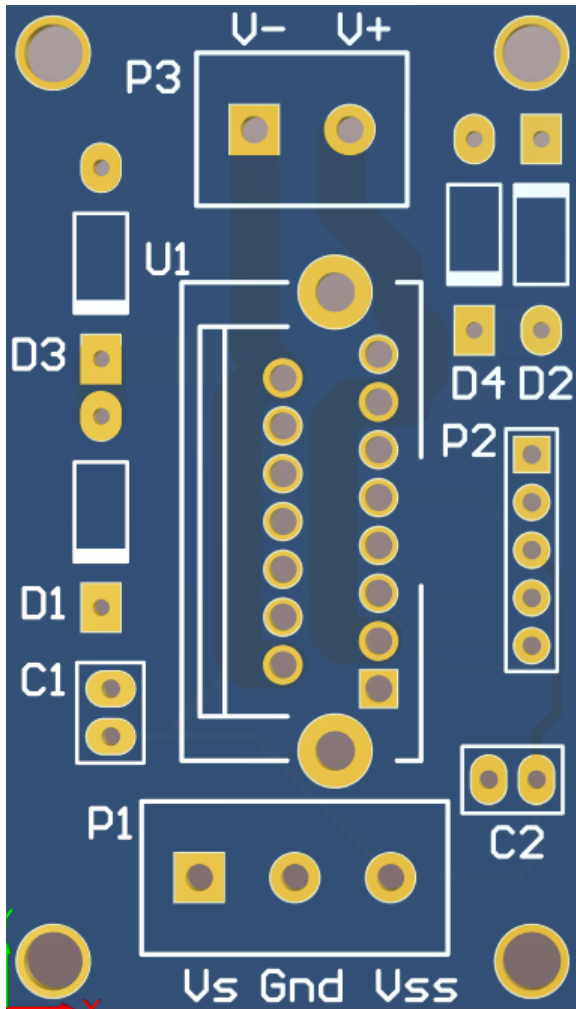
Rat's nests indicate connectivity as per schematic (Net names are assigned to part terminals)

All parts in the schematic with their selected footprints

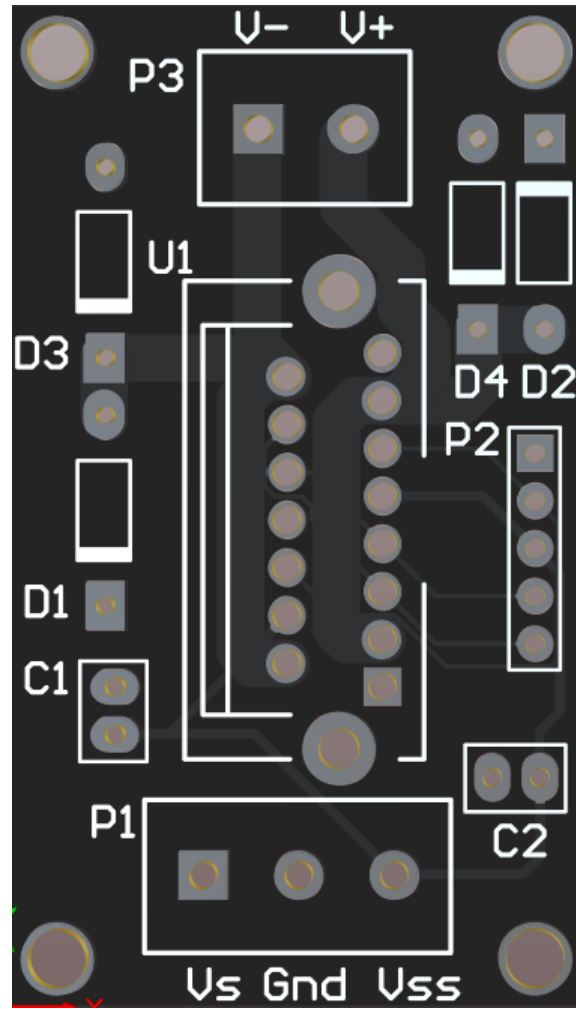
Top Layer Bottom Layer Mechanical 1 Top Overlay Bottom Overlay Top Paste Bot Snap Mask Level

PCBs are multi-layer entities

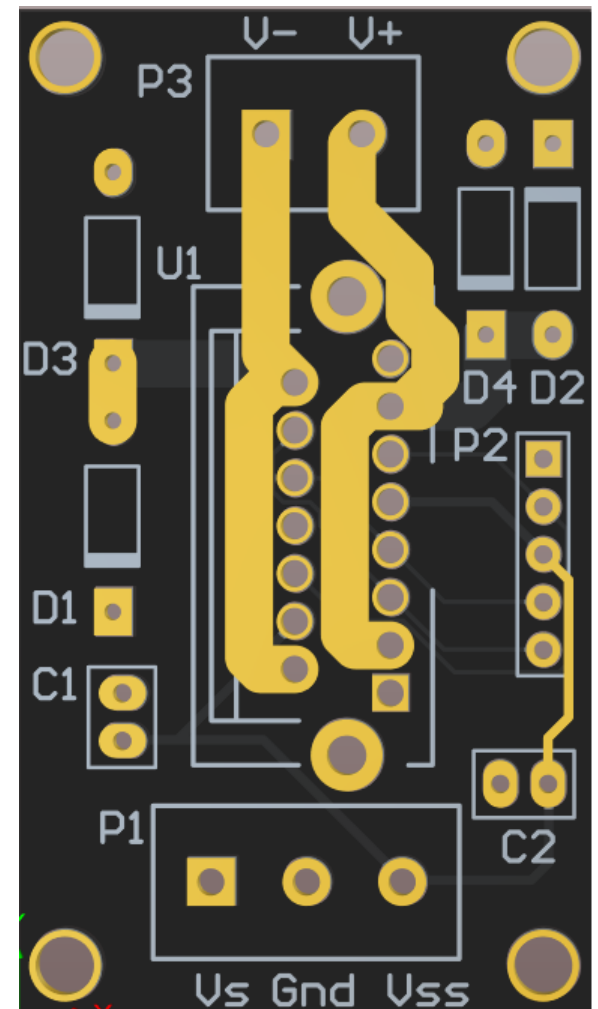
Top view all layers



Top overlay layer



Top copper layer

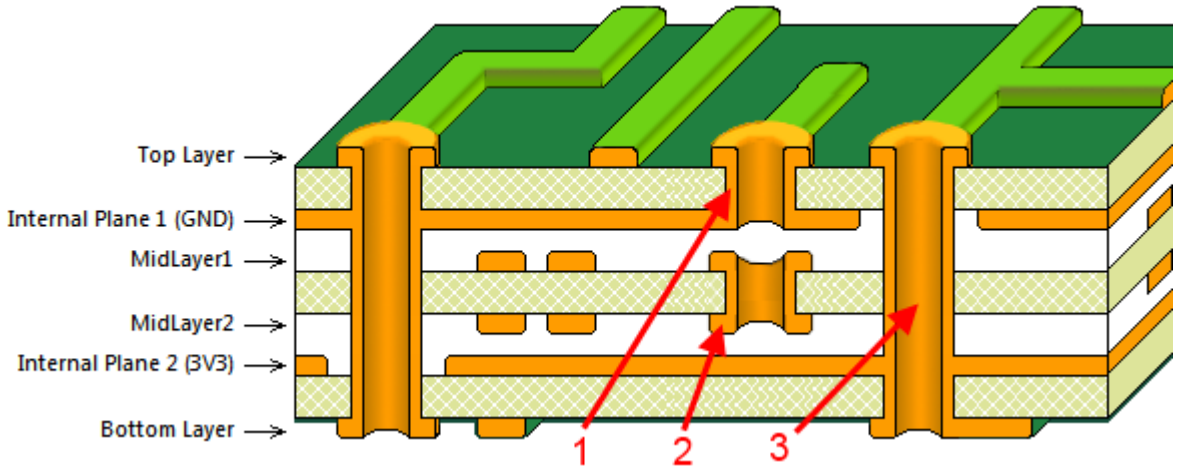
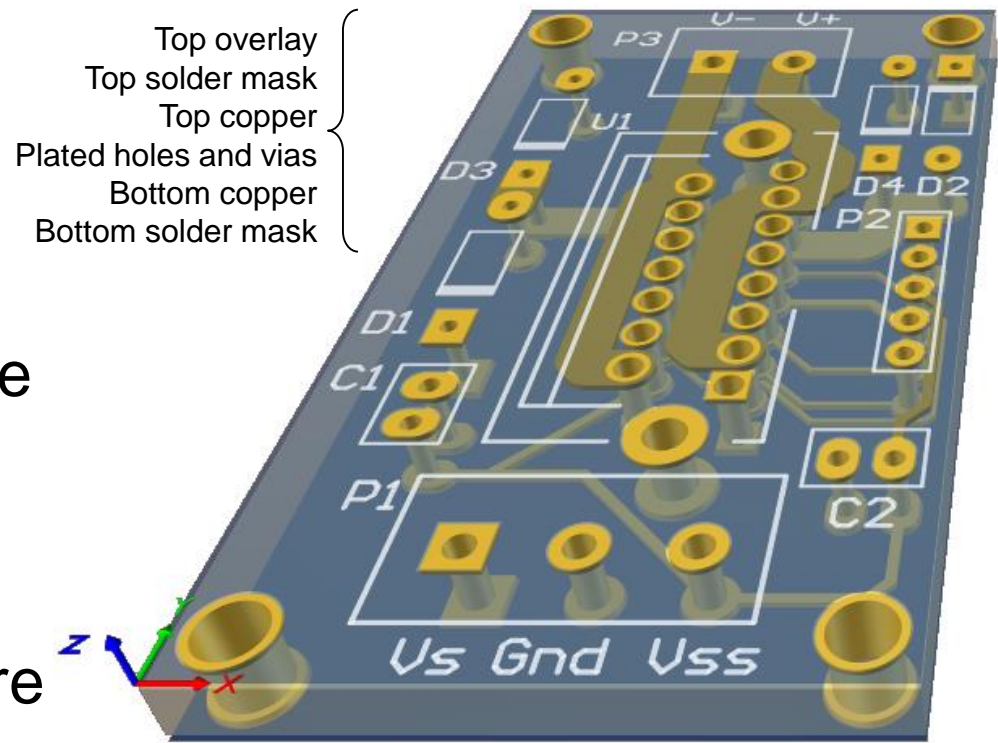


This is a 2 layer PCB

1 dielectric substrate with top and bottom copper

You as a designer specify the location of objects and features of every layer

Holes, vias, and footprints are grouped multi-layer objects



More complex PCBs have a stack-up of multiple boards and hence more layers

PCB Laminates

- Substrate (laminate)

- Rigid board of insulating material, provides structural support.
- Available in different materials and thicknesses, e.g:
FR4, Rogers/Duroid, Teflon (PTFE) 8mils (0.2mm) → 240mils(6.1mm)
- Most commonly used material type is FR4, 62mils thick
- Available with different copper thicknesses

Cu thickness measured in weight oz/ft²

½ oz → 0.7mils

1 oz → 1.4mils

2 oz → 2.8mils

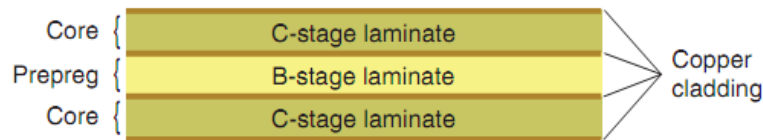


Figure 1-3 Cores and prepreg.

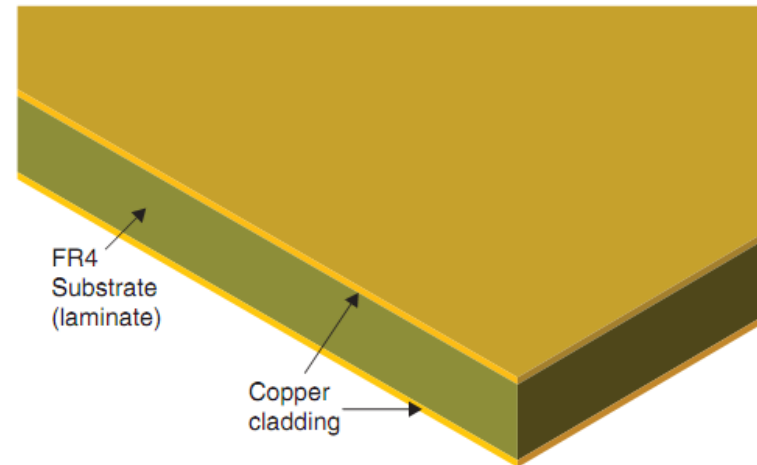


Figure 1-2 A double-sided copper clad FR4 substrate.

PCB Anatomy: Layer Stackup

Design >> Layer Stack Manager ...

This will enable additional layers as required

Information on substrate thickness, type and dielectric is not included in Gerber CAM files, these need to be explained separately to the manufacturer.

Layer Stack Manager

Save... Load... Presets Measurement Unit Imperial

	Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
	Top Overlay	Overlay						
	Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
1	Top Layer	Signal	Copper	1.4				Top
	Dielectric 1	Dielectric	None	12.6	FR-4	4.8		
2	Bottom Layer	Signal	Copper	1.4				Bottom
	Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
	Bottom Overlay	Overlay						

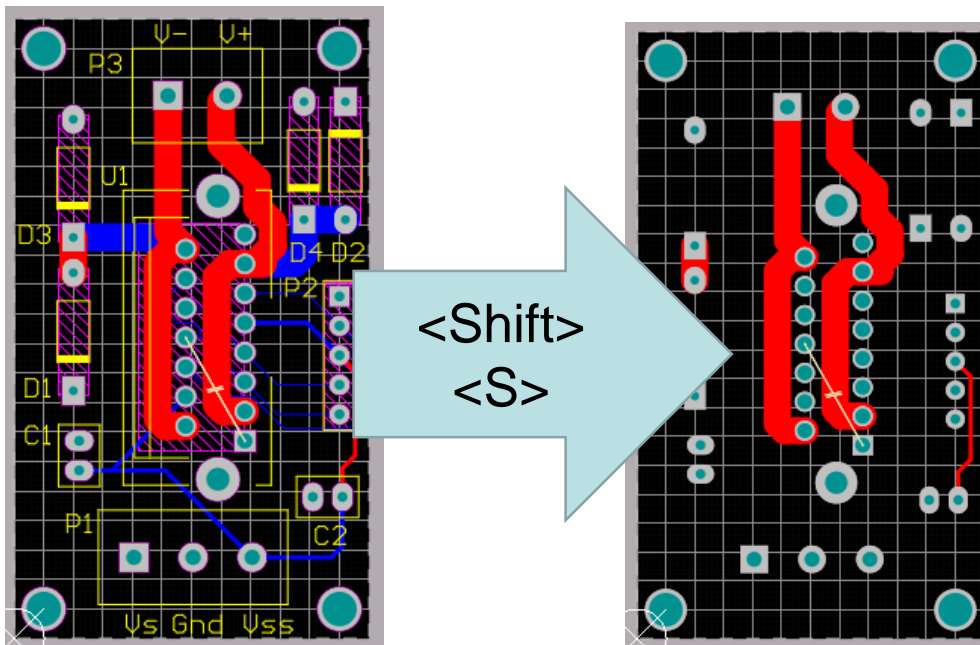
This is a two-sided board with only: Top Layer & Bottom Layer

Working with Layers

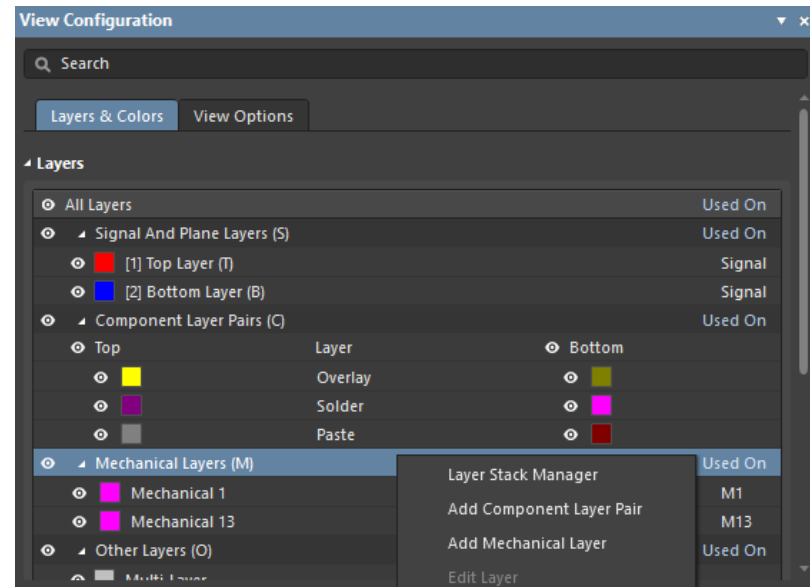
- Use the tabs at the bottom of the editor to switch between layers



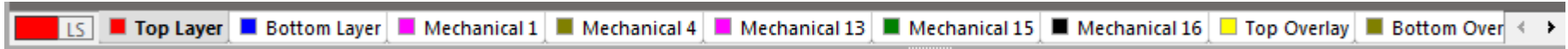
To switch to single layer mode



To set relevant layers
View » Panels » View Configuration
or press <L>



Configuring the Display Layers

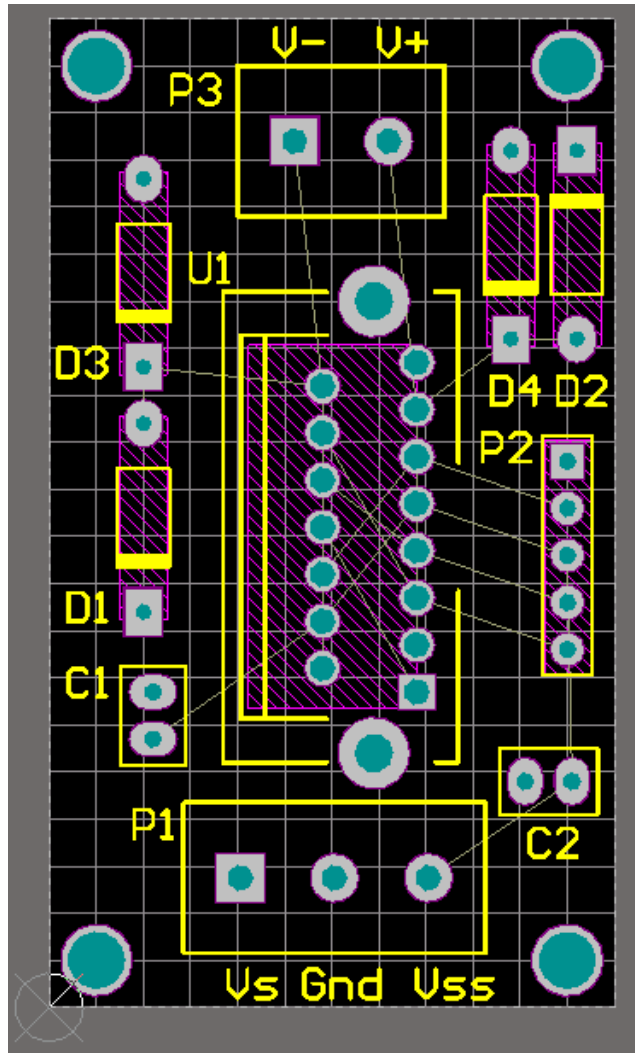


- **Electrical layers**
32 signal layers and 16 internal power plane layers.
- **Mechanical layers**
32 general purpose mechanical layers, used for design tasks such as dimensions, fabrication details, assembly instructions, or special purpose tasks such as glue dot layers. These layers can be selectively included in print and Gerber output generation. They can also be paired, meaning that objects placed on one of the paired layers in the library editor, will flip to the other layer in the pair when the component is flipped to the bottom side of the board.
- **Special layers**
these include the top and bottom silkscreen layers, the solder and paste mask layers, drill layers, the Keep-Out layer (used to define the electrical boundaries), the multilayer (used for multilayer pads and vias), the connection layer, DRC error layer, grid layers, hole layers, and other display-type layers.

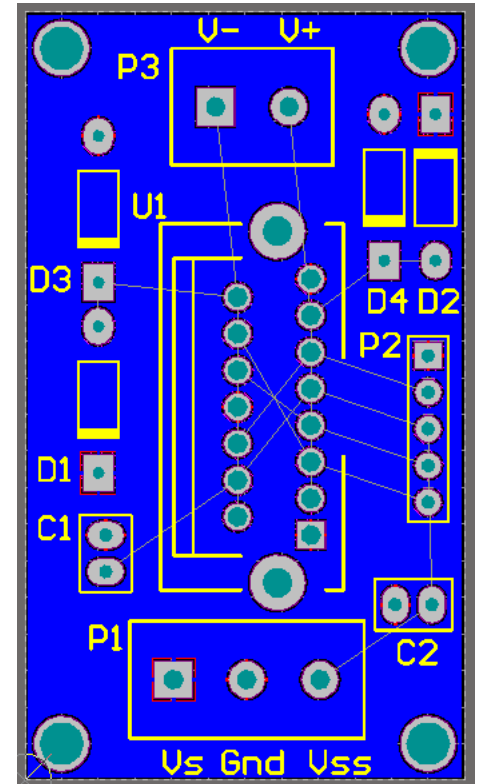
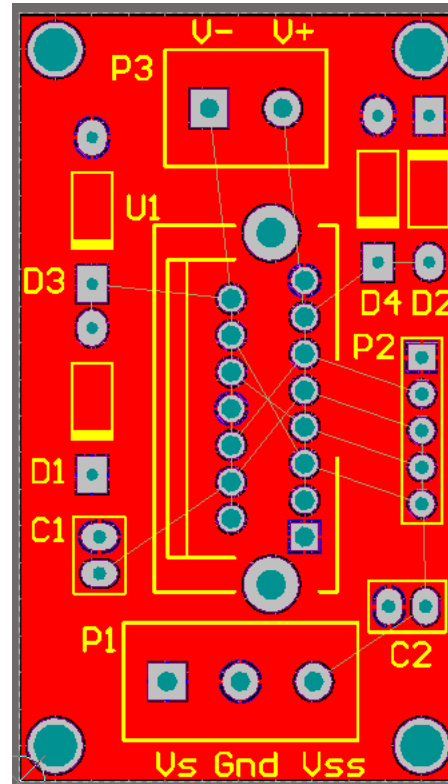
Mechanical Layers

- Multi-purpose layers
- E.g. Altium supports 32 Mechanical layers: M1 ... M32
- Typically
 - M1 Board outline
 - M2 PCB manufacturing info
 - M11-M12 Top and bottom layer dimensions
 - M13 Top layer 3D models and mechanical outlines
 - M14 Bottom layer 3D models and mechanical outlines
 - M15 Top layer assembly information
 - M16 Bottom layer assembly information

Positioning components & routing

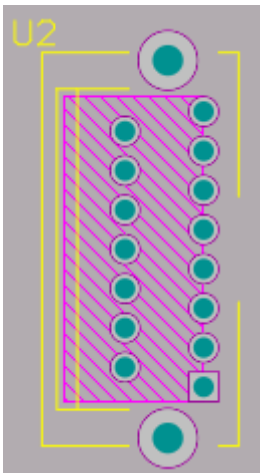


Place a plane on top for GND
Place a plane bottom for V_s



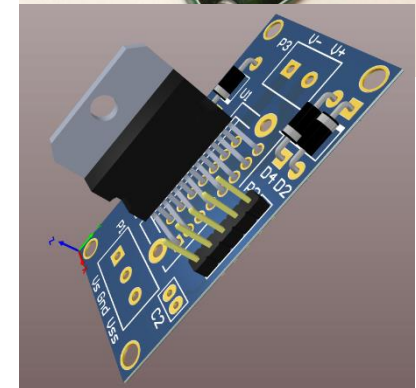
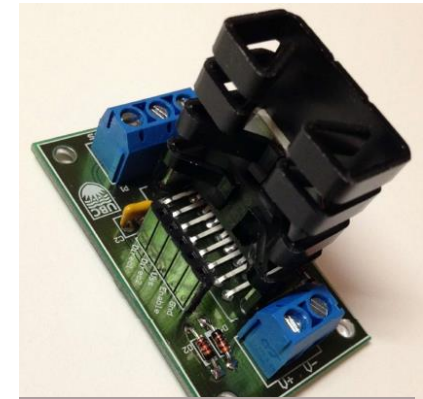
Positioning components & routing

- When placing components:
 - Try to align parts (same orientation)
 - Ensure that labels are all set in the same direction
 - Beware of bulky connectors (use 3D view with caution)



Yellow (top overlay) lines in footprints typically mark the physical boundaries of a part. However, you must be cautious and think about it.

This footprint includes the space taken by a heatsink, but does not show it in the 3D view.



About Traces / Tracks

- Copper traces are patterned either by:
 - Photolithography: requires photomasks
 - Laser: used to draw patterns on photoresist
 - Mechanical milling: Cu is removed to isolate the traces.
- Trace width and thickness determines:
 - Ampacity (current carrying capacity)
 - Characteristic impedance for RF designs
- Practical limitations:
 - Minimum trace width and gap for e.g. 7mils/7mils is typical fab. spec.

Negative view:
Copper planes, Drill
holes, Solder Masks



Figure 1-18 Copper in a plane layer (negative view without drill info). (a) Copper plane with thermal relief. (b) Negative view in Layout.

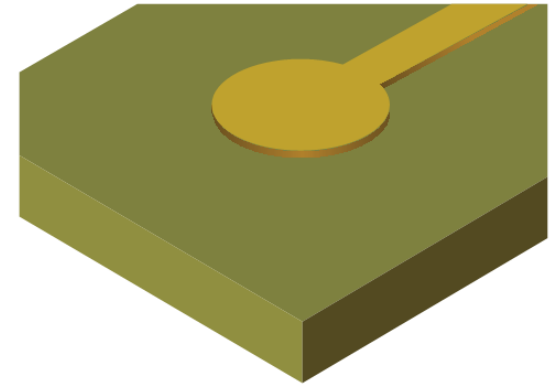


Figure 1-11 Copper pad and trace after etching and resist stripping.

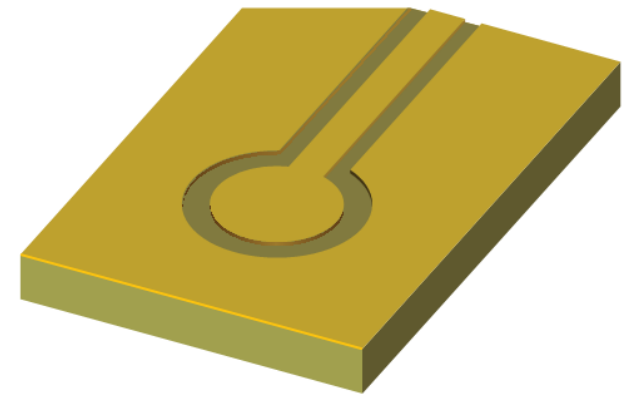
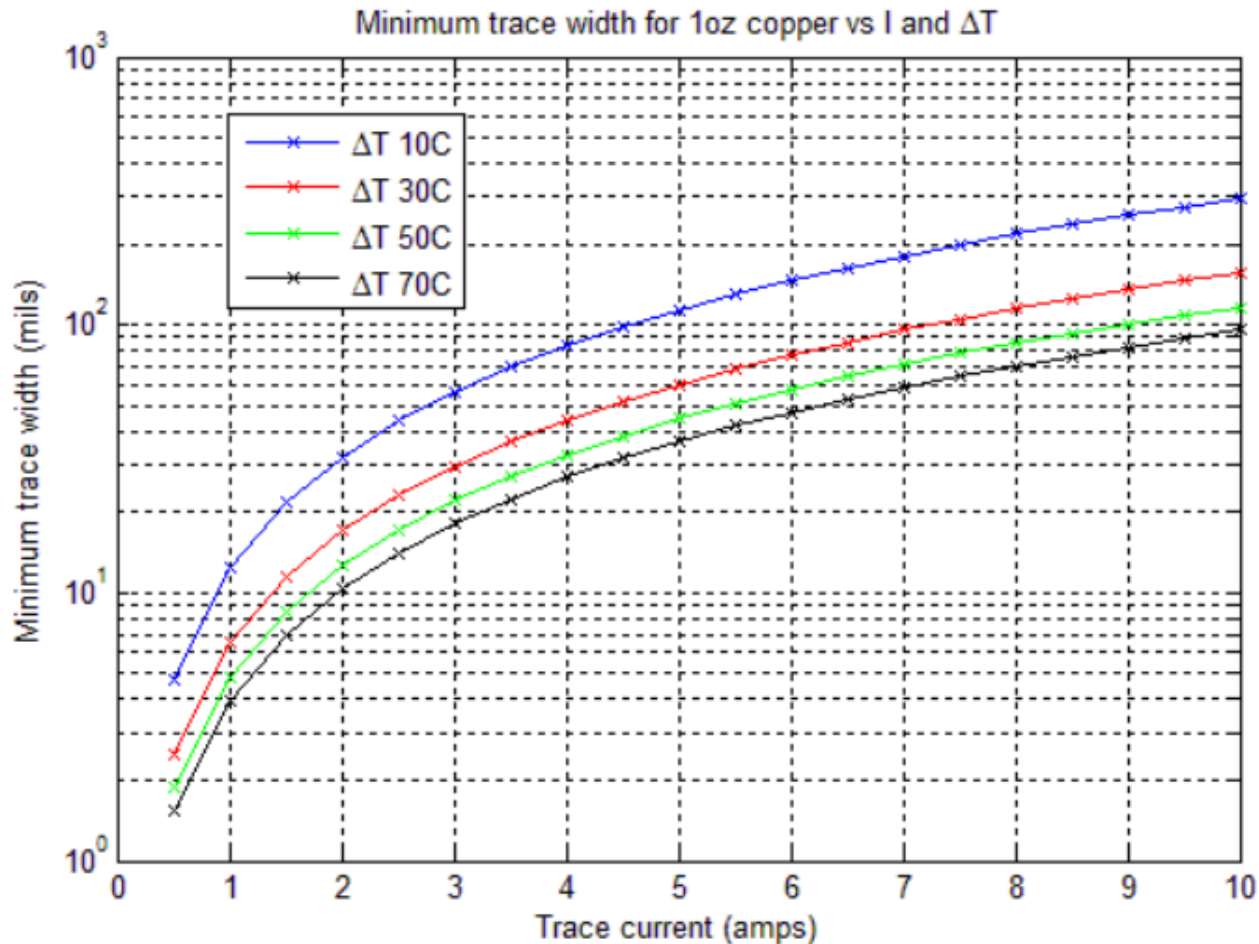


Figure 1-12 A mechanically milled trace.

Determining trace width



Use the following online trace width calculator:

<http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator>

Handy shortcuts for routing

- Press * on the numeric keypad while routing to cycle through the available signal layers. A via will automatically be added, in accordance with the applicable Routing Via Style design rule. Alternatively, use **Ctrl+Shift+Roll** shortcuts to move back and forth through the available signal layers.
- **Shift+R** to cycle through the enabled conflict resolution modes, including Push, Walkaround, Hug and Push, and Ignore. Enable the required modes in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.
- **Shift+S** to cycle single layer mode on and off, ideal when there are many objects on multiple layers.
- **Spacebar** to toggle the corner direction (for all but any angle mode).
- **Shift+Spacebar** to cycle through the various track corner modes. The styles are: any angle, 45°, 45° with arc, 90° and 90° with arc. There is an option to limit this to 45° and 90° in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.

Design Rules

- Design >> Rules

Rule	Constrain	Query
Electrical, Clearance	Min clearance = 7mil	All
Routing, Width*	Min width = 7mils Max width = 500mils Preferred = 10mils	All
Routing, Width_IO	Min width = 7mils Max width = 500mils Preferred = 100mils	Advanced (Query) (InNet('V+') OR InNet('V-'))
Width_Vss	Min width = 7mils Max width = 500mils Preferred = 20mils	Net Vss

Custom Routing design rules

The screenshot shows the PCB Rules and Constraints Editor with a custom routing rule named "Width_1" selected. The rule is configured with a name of "Width_1", a unique ID of "EWBDPXHU", and a "Test Queries" button. The "Where The Object Matches" section is set to "All". The "Constraints" section includes a diagram of a yellow track with a width of 10mil and a "Max Width 10mil" label. The "Check Tracks/Arcs Min/Max Width Individually" option is selected. The "Attributes on Layer" table is shown below.

Attributes on Layer			Layer Stack Reference		Absolute Layer	
Min Width	Preferred Size	Max Width	Name	Index	Name	Index
10mil	10mil	10mil	10mil Top Layer	32	TopLayer	1
10mil	10mil	10mil	10mil Bottom Layer	33	BottomLayer	32

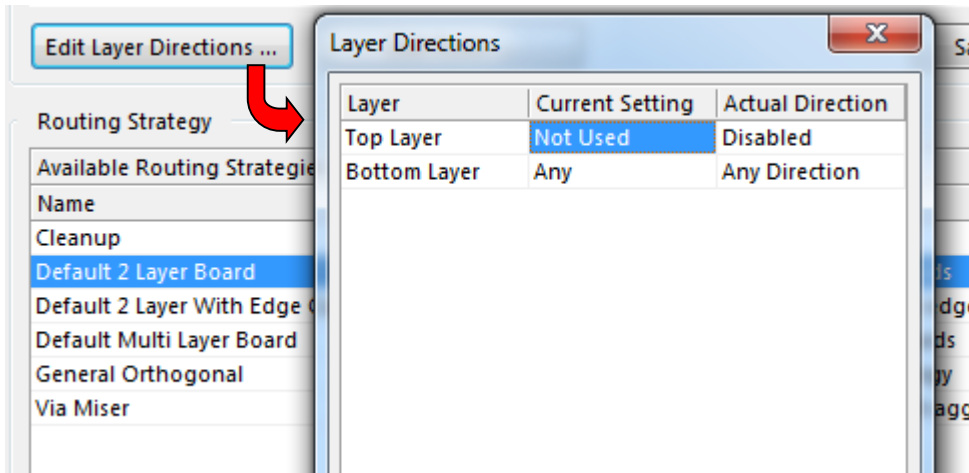
Rename to "Width_IO"

Use 'Custom Query' to set"
Belongs to net V+
OR
Belongs to V-

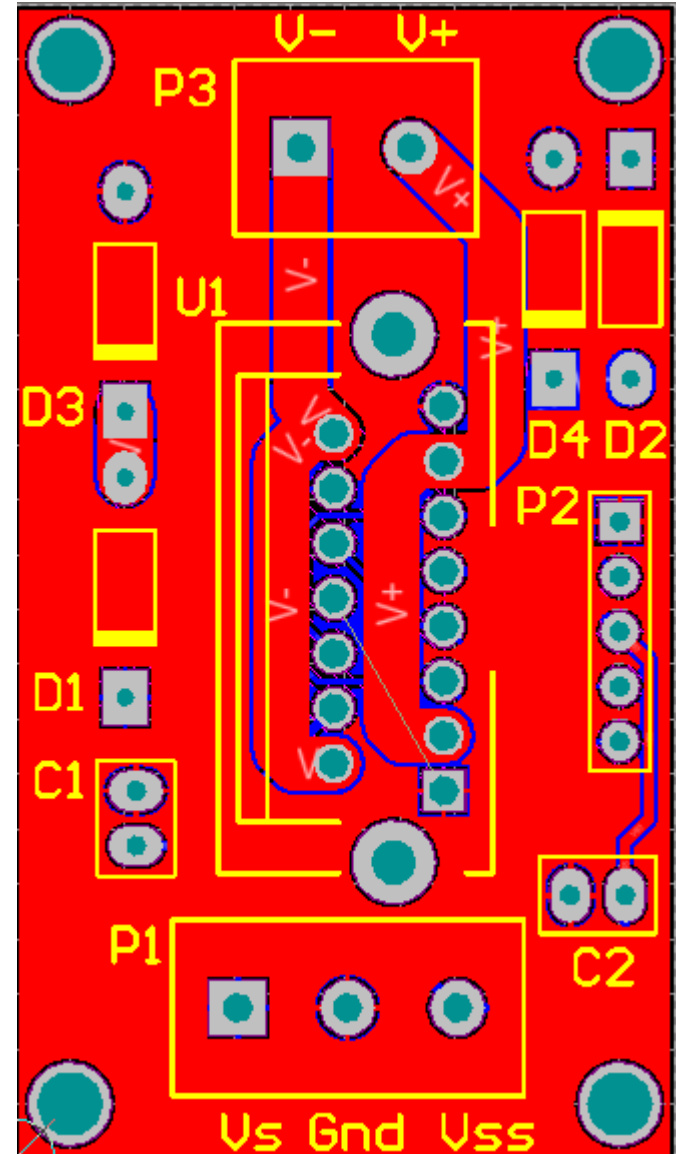
Set rule execution
priority

Auto route

- Rout » Un-Route » All
- Auto Route » All



- You can also set single layer routing



Holes

Holes can be:

- Vias, multi-layer pads, mounting holes, or cuts
- Plated or non plated

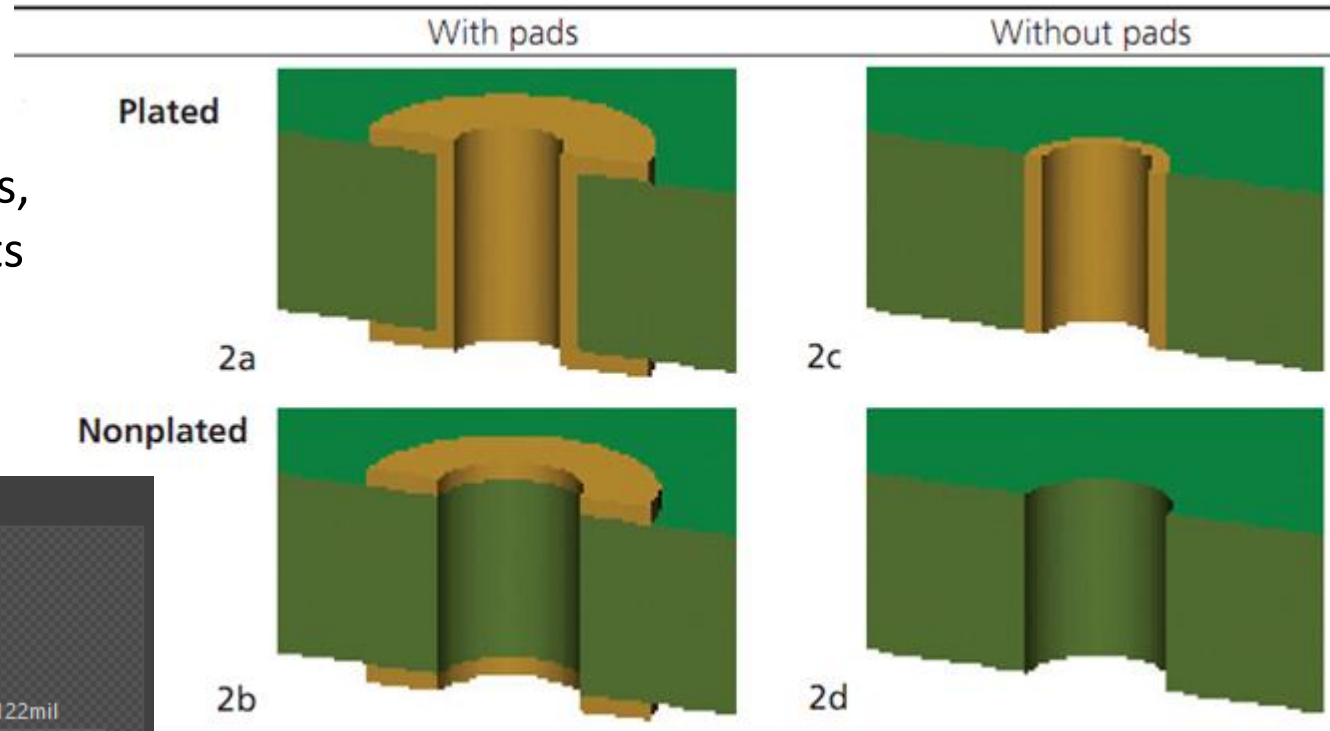
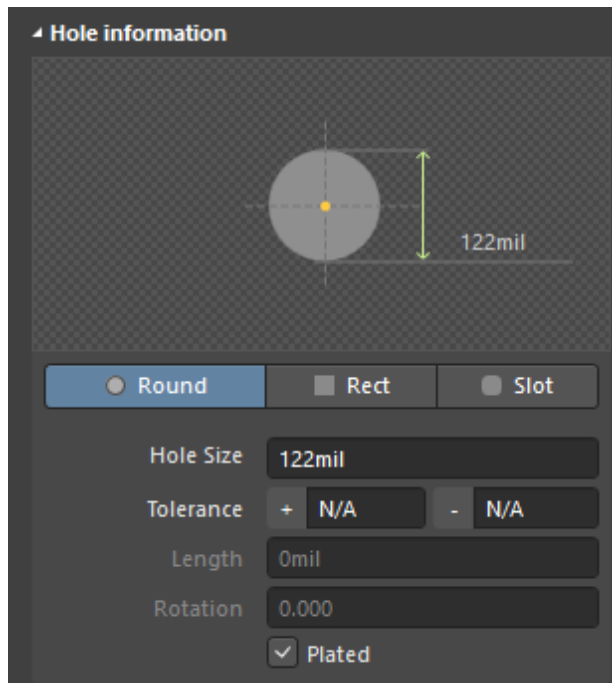


Table 8-2 Basic hole types

You must specify whether a hole is plated or non plated during the design process

Plating reduces hole size by 0.003"

Hole sizes

- Common hole sizes: non-plated vs. plated sizes

Drill Number Set	Drill Size	Finished Size	Approximate Use
#76	.020"	.017"	via holes
#70	.028"	.025"	via holes, fine lead devices such as trim pots etc.
#65	.035"	.032"	IC's, 1/4 watt resistors, small diodes, ripple caps etc.
#62	.038"	.035"	Square posted pins that measure .025" on the flat.
#58	.042"	.039"	TO-220 packages, IDC type square posted headers, 1/2 watt resistors, 1N9000 series diodes, IC chip carriers, etc.
#55	.052"	.049"	larger connectors, transformer leads, etc.
#53	.060"	.057"	similar to .052" above
#44	.086"	.083"	TO-220 mounting holes, screw holes, general mounting
1/8 in.	.125"	.122"	mounting holes
#24	.152"	.149"	mounting holes

Vias

- Connection between layers is accomplished with via holes
- After the holes are drilled, their inner walls are plated
- Top and bottom traces are patterned after plating

Source: wikipedia.org: Thermal pad

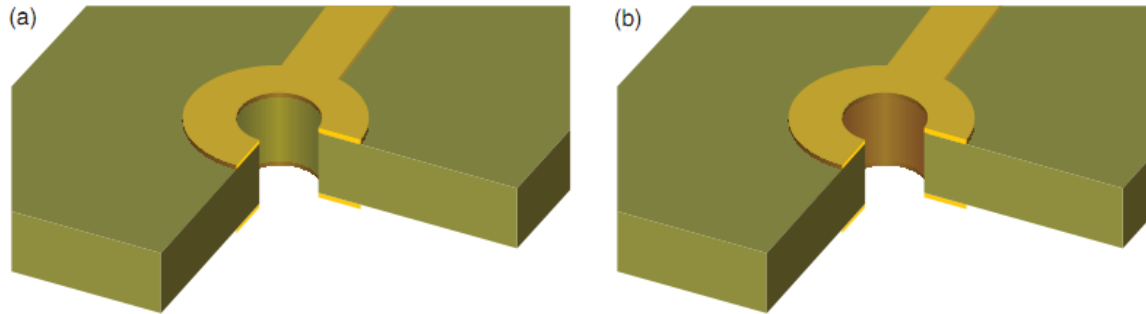
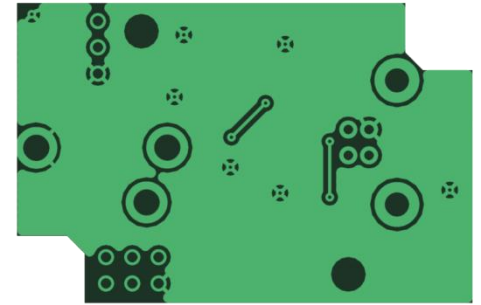
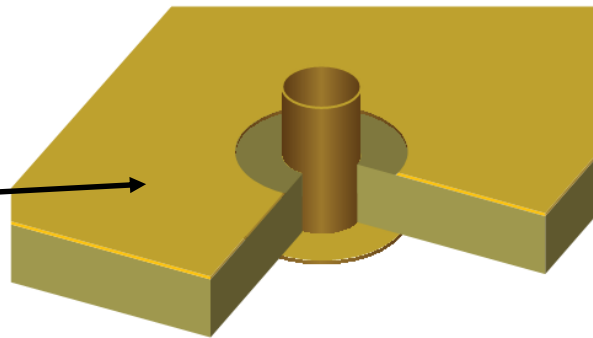


Figure 1-13 Holes are drilled into the board and then copper plated. (a) A nonplated through-hole. (b) A plated through-hole.

Thermal relief is needed when connecting a via to a copper plane

PWR and GND planes are commonly inner layers



Teardrops:

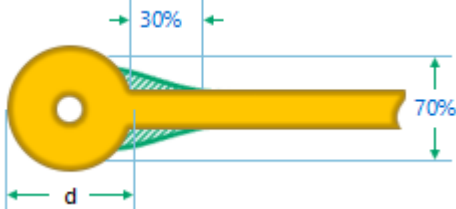


Figure 1-15 A clearance area provides isolation between a plated hole and a plane.

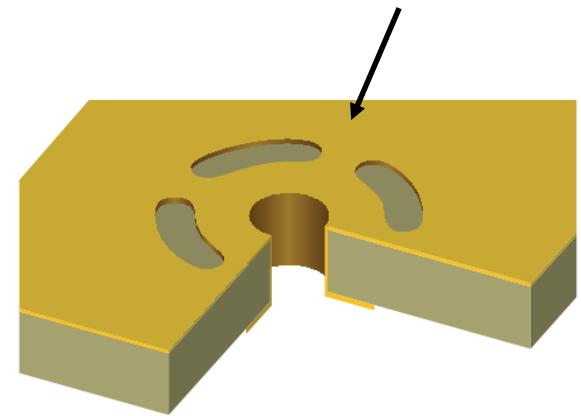


Figure 1-14 A connection to a plane layer through a thermal relief.

Types of Vias

- Types of via holes:
 - Plated and un-plated through-hole, blind, buried

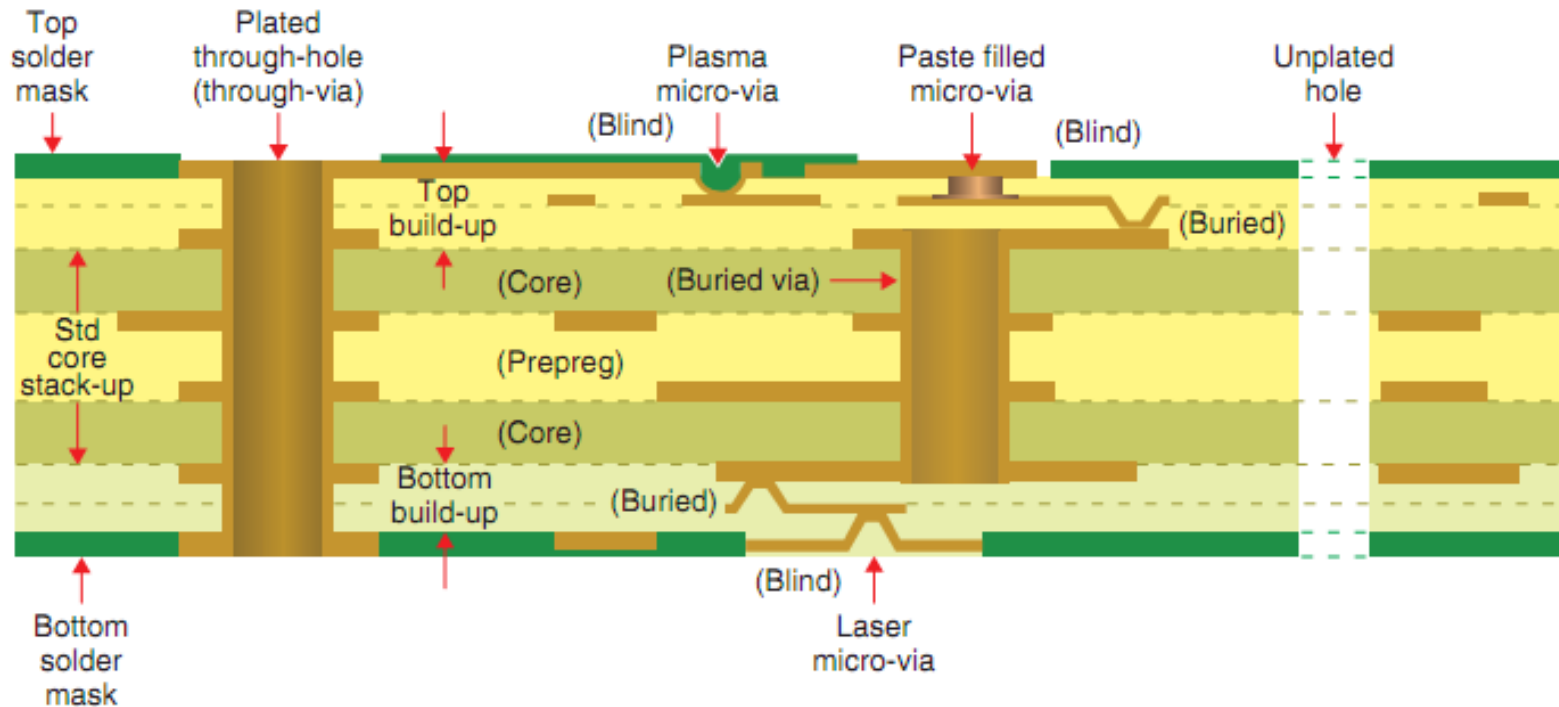


Figure 1-5 A built-up, multitechnology, PCB stack-up.

Solder mask

- Solder mask or solder resist:
 - Thin polymer layer deposited on top and bottom layers
 - Protects outer layers from oxidation and prevents solder bridges
 - Allows for wave or reflow soldering of components
 - Holes are opened with photolithography wherever components will be soldered
 - Default color is green, but any other color is possible

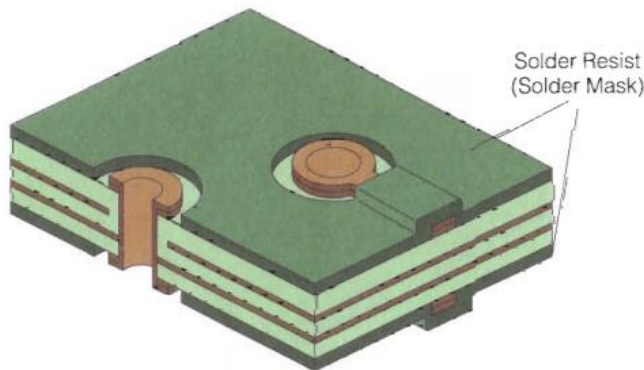


Illustration ML-14. *Apply solder resist.* The specified resist (either dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.

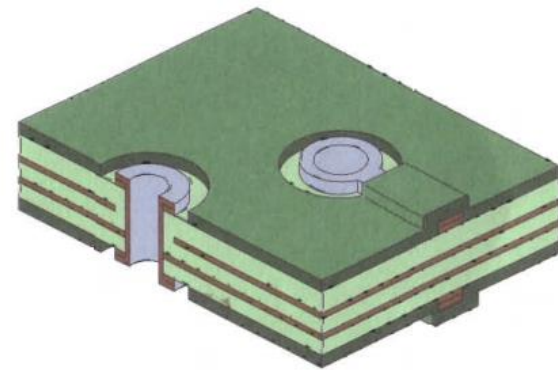
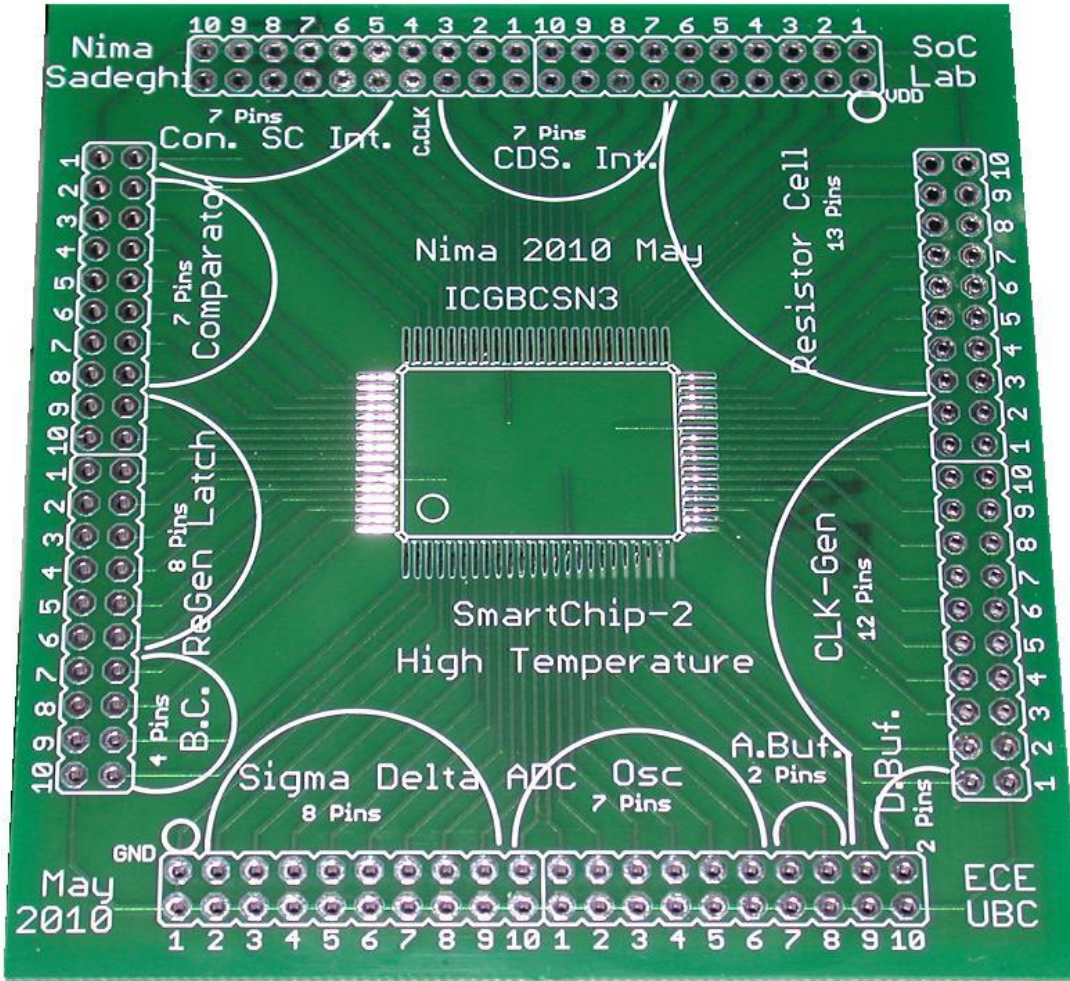


Illustration ML-15. *Solder coat.* Solder (tin/lead) is applied to the exposed copper areas, and the excess solder is removed.

Source: Printed Circuit Board Basics: An Introduction to the PCB Industry, by: Michael Flatt

Legend / Silkscreen / Overlay



- Legend or silkscreen:
 - Applied on top of the solder resist
 - Can be applied to one or both outer layers
 - Default color is white but any other color is possible

Tip: add (Top) and (Bottom)

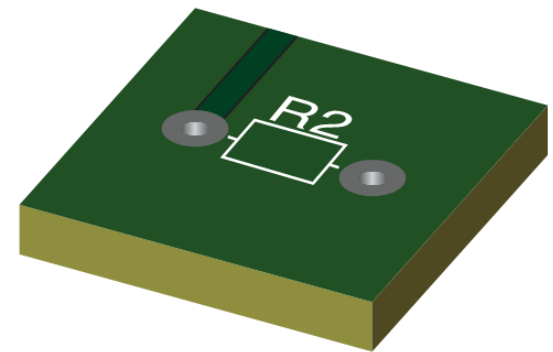


Figure 1-16 Final layers are the soldermask (green) and silk screen (white).

Instructions for ELEC391 fabrication submissions

Submission Instructions

- No limits to # of boards (7 deadlines)
- Cost: \$25 + \$10/ sq-in, from project budget
- Submission dates:

Midnight, Mondays

Feb 3, Feb 10, Feb 17, Feb 24,

Mar 2, Mar 9, Mar 16

we will check submissions and accept fixes
until 5PM the following Tuesday

M	T	W	Th	F	Sa	S
M	T	W	Th	F	Sa	S

- Turn around: 5-6 business days
- Work within the given guidelines
- Verify PCB layout and design - prior to design submission
- Submissions will be rejected if guidelines are not followed

An aerial view of a green printed circuit board (PCB) panel. The panel is divided into several rectangular sections, each containing a different circuit board design. The designs are printed in white and include various components, traces, and labels. Some sections show complex multi-layer designs with numerous components, while others show simpler designs with fewer components. The panel is oriented vertically, and the designs are arranged in a grid-like pattern. The text "We will panelize your designs to speed up fabrication and reduce costs" is overlaid in the center of the image.

We will panelize your designs to speed up fabrication and reduce costs

Panelized designs from elec391 Spring 2016

Submission Instructions

- You can send several different boards per submission
- You can request several copies of each but that increases your area & cost
- Email pcb@ece.ubc.ca
Subject: [PCB] ELEC391, Group #, submission#
- Attach: Zipped file with your PCB Project file (*.PrjPcb) and all associated files, also include the latest DRC report.
(make sure all files are under the same directory)

Body:

Total number of boards to fabricate:

Name of boards to fabricate and number of copies for each

Design constrains 1/2

1) Layers:

- 1) Maximum number of electrical layers = 2
- 2) Bottom overlay (PCB underside text) will not be manufactured - please use "bottom layer" for bottom text

2) Try to minimize the size of your PCB

Components can be placed side by side (recommend 50-100 mil IC's separation for most cases)

3) Do not forget to:

Add your group number on the top overlay – make it visible

Draw a board outline on layer “Mechanical 1”

if several boards in a single file, draw a board outline for each
(min spacing from edge of board for any feature is 10mils)

Design constrains 2/2

- 4) Install provided Design-Rules file (available [here](#)) please do not modify base rules, but you can add custom routing rules.
Submissions that do not pass DRC will be rejected

The screenshot shows the PCB design software interface. The 'Design' menu is open, and the 'Rules...' option is highlighted. A red circle with the number '1' is placed over the 'Rules...' menu item. The 'PCB Rules and Constraints Editor [mil]' window is open, showing the 'Clearance' rule. A red circle with the number '2' is placed over the 'Clearance' rule. The 'Constraints' section shows a diagram of a track and a via with a minimum clearance of N/A. A red circle with the number '3' is placed over the 'Constraints' section. The 'Design Rule Check...' dialog is open, showing the 'Reset Error Markers' button. The 'Tools' menu is open, and the 'Design Rule Check...' option is highlighted.

1

2

3

Project Place Design Tools Route Reports Window Help

Update Schematics in L298_Board.PrjPcb

Import Changes From L298_Board.PrjPcb

Rules...

PCB Rules and Constraints Editor [mil]

Design Rules

- Electrical
 - Clearance
 - Clearance
 - Short-Circuit
 - Un-Routed Net
 - Un-Connected Pin
 - Modified Polygon
 - Routing
 - Width
 - Width_Vss
 - Width_IO
 - Width
 - Routing Topology
 - Routing Priority
 - Routing Layers
 - Routing Corners
 - Routing Via Style
 - RoutingViaSize_17
 - RoutingViaSize_25
 - RoutingViaSize_32
 - RoutingVia
 - Fanout Control
 - Differential Pairs Routing
 - SMT
 - Mask
 - Plane
 - Testpoint
 - Fabrication Testpoint Style
 - Fabrication Testpoint Usage
 - Assembly Testpoint Style
 - Assembly Testpoint Usage
 - Manufacturing
 - High Speed
 - Placement
 - Signal Integrity

Name: Clearance Comment: Unique ID: CNOBFXK Text Queries:

Where The First Object Matches: All

Where The Second Object Matches: All

Constraints

Different Nets Only

Minimum Clearance: N/A

Ignore Pad to Pad clearances within a Footprint

Simple Advanced

	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	7					
SMD Pad	7	7				
TH Pad	7	7	7			
Via	7	7	7	7		
Copper	7				7	
Text	7					7
Hole	0					

Required clearance between largest of Electrical Clearance

Rule Wizard... Priorities... Create Default Rules

L298_Board.PrjPcb - A

Project Place Design Tools Route Reports Window Help

Design Rule Check...

Reset Error Markers

How to load design rule file

- DRC file and these same instructions from [here](#)
- Download and save as “.RUL” file
- On your PCB design select:
Design >> Rules
- On the 'PCB Rules and Constrains Editor', Right click anywhere on the left column
 - Select: Import Rules
 - Select all rules in window (using shift and mouse or <Ctrl> +<A>) → OK
 - Browse to select .RUL file
 - Clear existing rules prior to import? → NO

Rules – design rules

- Component clearance and (electrical) clearance:
 - Minimum distance = 7 mil
- (Routing) width:
 - Minimum trace width = 7 mil
- Annular ring size:
 - Minimum annular ring size = 7 mil
 - Minimum annular ring size for vias = 5 mil
- Board outline clearance: 10mils
- No limit to allowed hole sizes

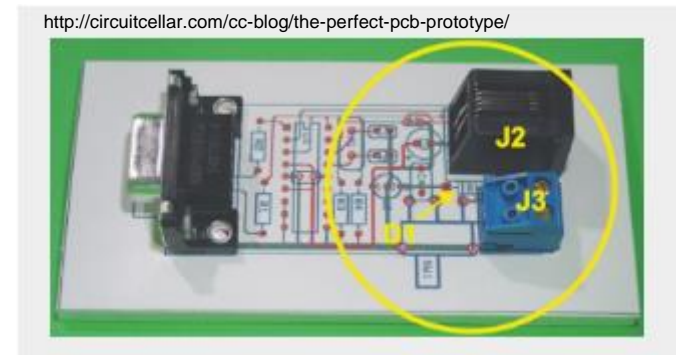
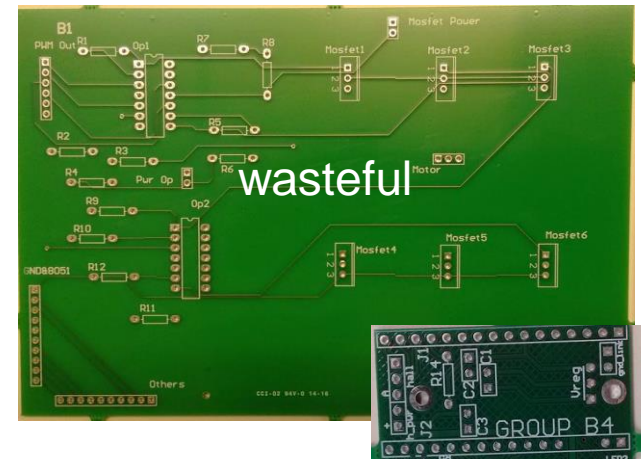




PCB Design Best Practices

Best Practices: Estimating board size

- Before starting layout it is good to have an idea of the target size of the PCB board and all other relevant dimensions.
- It is very helpful to have the components at hand to plan the floor-plan.
- An old good trick of the trade is to print the PCB layout at a 1:1 scale, place the printout on a foam and stick on the through hole components.

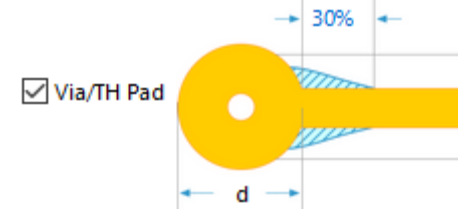


Best Practices: Floor planning

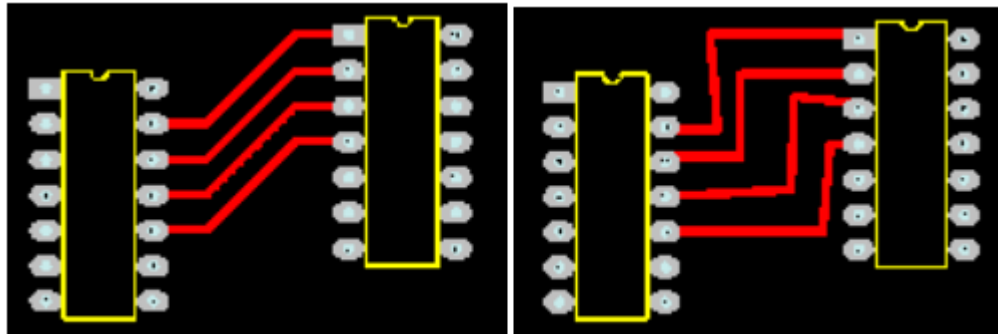
- Choose your units and set the grid
- Carefully plan the placement of components
 - Place analog and digital sections apart
 - Group components into 'functional blocks'
 - Place ICs in the same direction
 - Align ICs, resistors, labels, capacitors etc.
 - Place de-caps close by their ICs
 - Place Op-amp resistors near the Op-amp
 - Plan for mounting holes and heat sinks
- Aim for symmetry when possible
- Do use Design Rule check

Best Practices: Routing strategy

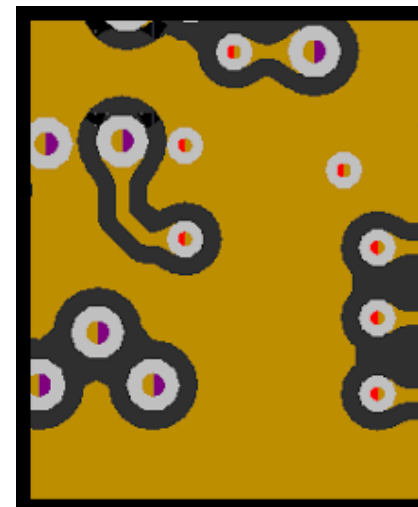
- On two sided boards keep traces perpendicular as much as possible
- Avoid 90 degree bends in tracks (reduced chances of acid traps)
- Keep traces as short as possible
- Always connect a trace to the center of the pad
- Use teardrops (Tools >> tear drops), and use vias to avoid lockout
- Do not place vias under SMD pads
- Layout first all critical traces
 - e.g. CLK, diff pairs, controlled length
- Polygons as fills:
 - Connect to GND (EMC), or do not leave 'dead copper'
- Rout nicely



[Ref 3]

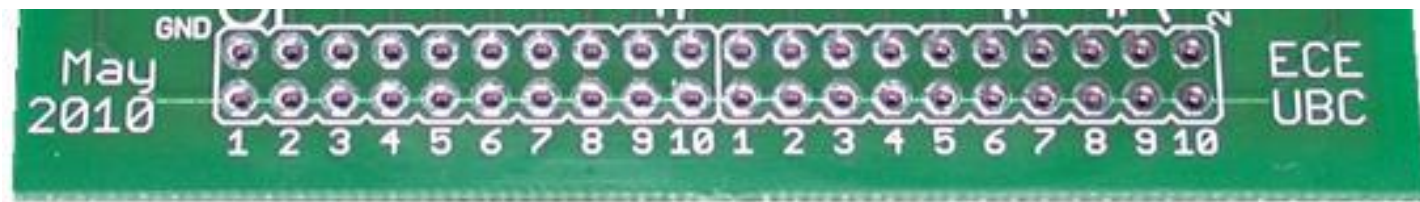


An example of GOOD routing (Left) and BAD routing (Right)



Best Practices: Labelling

- Always sign your design: add date, version, and name of board
- Label all relevant inputs and outputs
- Default sizes for comments and designators are 60mils x 10mils
- If you have silkscreen on both sides add a 'TOP' label to the top overlay.



Best Practices: Finishing touches

- Add mounting holes
- Confirm Board Information
 - *Properties panel: Board information* section (when no objects are selected)
 - Click on *Reports* and select:
 - Board Specifications
 - Non-Plated Hole Size
 - Plated Hole Size
- Using the hole size editor:
 - Minimize the total number of holes sizes
 - Verify that all vias are the same size (if possible)
- Verify that there are no unwanted leftovers on any Mechanical layer

Online resources

1. [Ten best practices of PCB design – EDN Magazine, Edwin Robledo & Mark Toth](#)
2. [Circuit Board Layout Techniques – Texas Instruments, Chapter 17 of Op-amps for everyone](#)
3. [PCB Design Tutorial – David L. Jones](#)